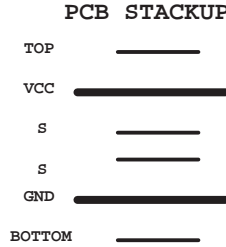
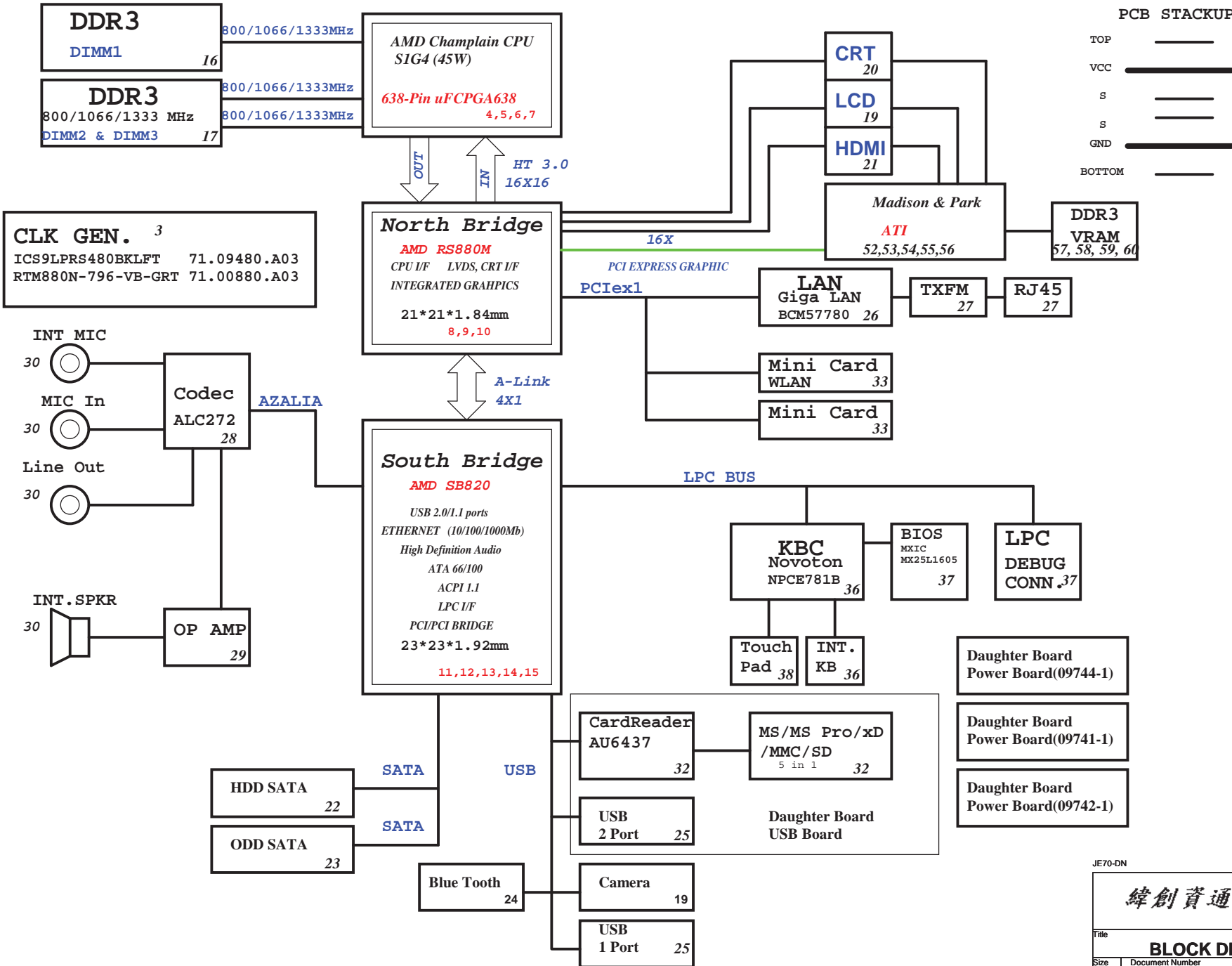


JE70-DN/SJV71-DN/HM72-DN Block Diagram

Project code: 91.4HP01.001
PCB P/N : 48.4HP01.011
REVISION : 09929-1



SYSTEM DC/DC RT8223 45	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8015A 47	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

RT9025 48	
5V_S5	1D05V_S0

RT9161 48	
3D3V_S0	2D5V_S0 (200mA)

RT9025 48	
3D3V_S0	1V_VGA (1.2A)

RT9025,RT8209E 47	
3D3V_S5	1D1V_S5
5V_S5	1D1V_S0

CHARGER BQ24745 49	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A
	VCC_CORE_S0_1 0~1.55V 18A
	VDDNB 0~1.55V 18A

EC Functional Strap Definitions

page9

STRAP_DEBUG_BUS_GPIO_ENABLEb Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#) *1 :Disable 0 : Enable
RS780: Enables Side port memory (RS880 use HSYNC#) *1 :Disable 0 : Enable
SUS_STAT# Selects Loading of STRAPS From EEPROM *1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

page15

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

page15

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	


NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

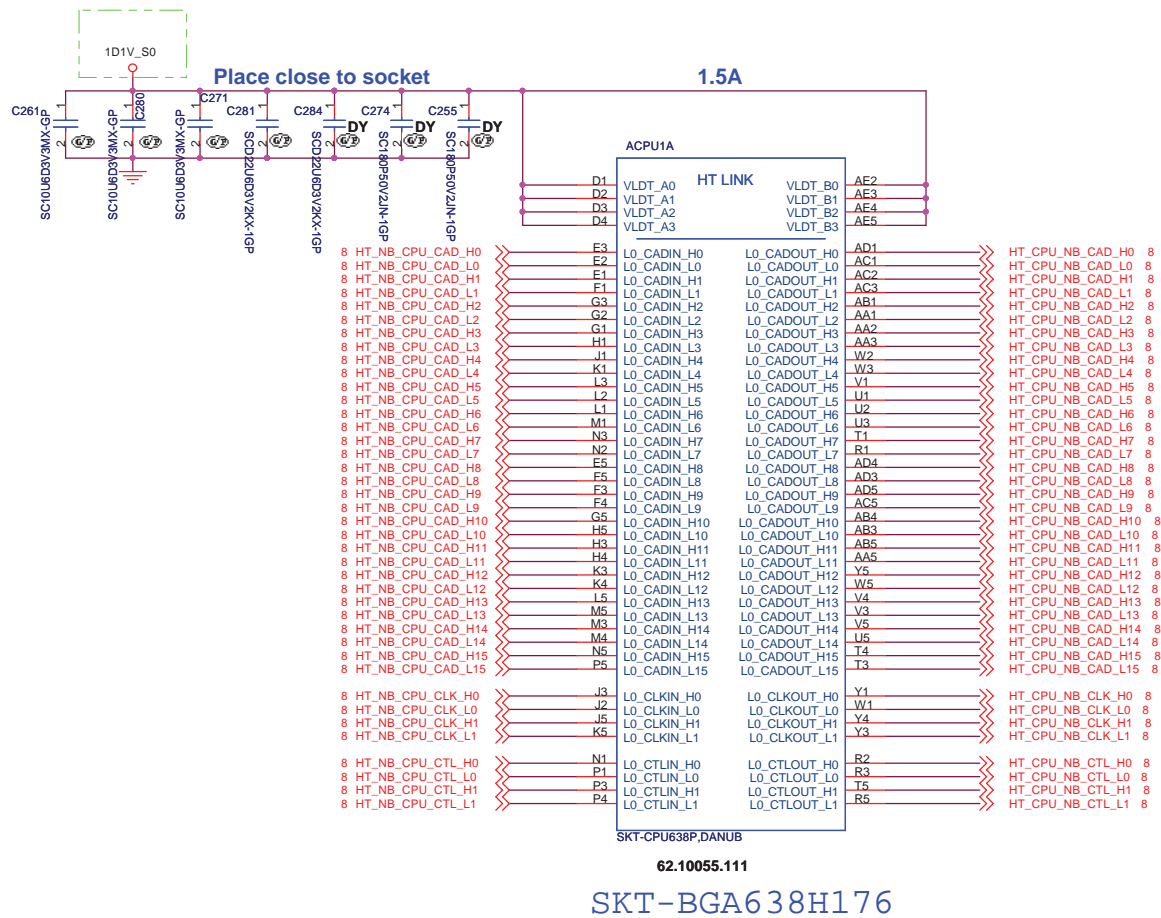
page12

	USB	
	Pair	Device
OCP3#	12	MINI2 CARD
	11	NC
	10	NC
	9	CCD
	8	NC
	7	Bluetooth
	6	USB3
	5	USB2
	4	CardReader
	3	NC
OCP2#	2	USB4
	1	MINI1 CARD
OCP0#	0	USB1

Signal	Comment
TEST# pin110	Test Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the device operation mode as follows: No pull-down resistor: Normal operation mode (XORTR and TRIST strap pins are ignored). 10 KΩ external pull-down resistor:Test mode (ICT or XOR-Tree Test mode, according to XORTR and TRIST strap pins).
XORTR# pin111	XOR-Tree Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the XOR-Tree Test mode, if TEST is strapped low: No pull-down resistor: Not allowed if TEST pin is strapped low. 10 KΩ external pull-down resistor:XOR-Tree Test mode .Note: TRIST strap pin must be left unconnected.
TRIST# pin112	ICT Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the ICT Test mode, if TEST is strapped low: No pull-down resistor: Not allowed if TEST pin is strapped low. 10 KΩ external pull-down resistor:ICT Test mode (see Section 3.4.1 on page 53), forces the device to float its output and I/O pins.Note: XORTR strap pin must be left unconnected.
JEN0#, JENK# pin49,53	JTAG Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the JTAG signals to device pins (see Table 4 on page 35 for details). Both JEN0 and JENK, are pulled to 1 by an internal resistor The external 10 KΩ pull-down resistor must be connected to GND.
SHBM pin83	Shared Host BIOS Memory. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the state of the shared BIOS memory. No pull-down resistor:Disable the shared BIOS memory. 10 KΩ external pull-down resistor:Enable the shared BIOS memory
SDP_VIS# pin41	Port80 (SDP) Visibility Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the Visibility mode for the Port80 (SDP). No pull-down resistor: SDP in Normal mode 10 KΩ external pull-down resistor:SDP in Visibility mode.
XOR_OUT pin35	XOR-Tree Output. The device pins are internally connected in a XOR-tree structure

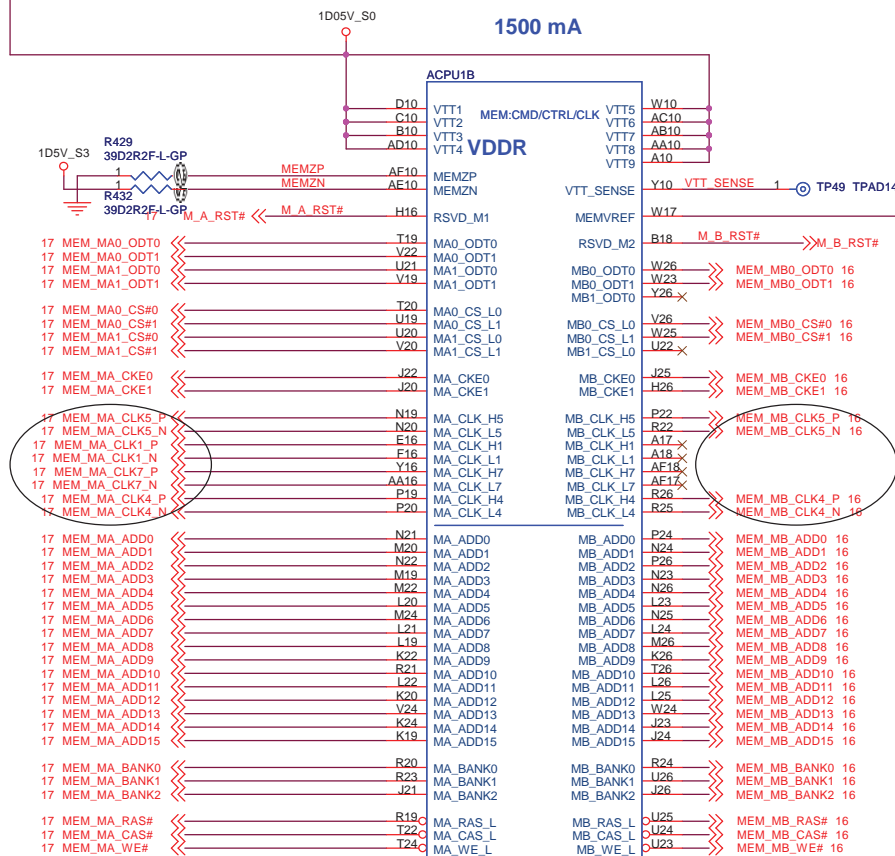
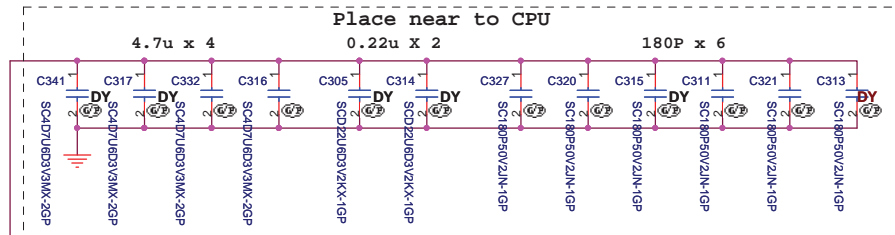
JE70-DN

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number JE70-DN
Date: Thursday, November 19, 2009	Rev SB
Sheet 2	of 63



JE70-DN

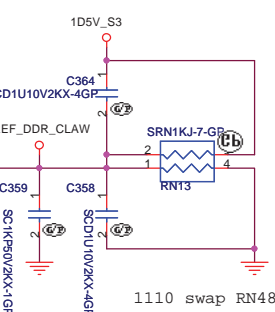
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<p>Title</p> <p>CPU HT LINK I/F (1/4)</p>	
<p>Size</p> <p>A3</p>	<p>Document Number</p> <p>JE70-DN</p>
<p>Date: Monday, March 01, 2010</p>	<p>Rev</p> <p>SB</p>
<p>Sheet 4 of 63</p>	



SKT-CPU638P,DANUB

62.10055.111

CLOSE TO CPU



1110 swap RN48



SKT-CPU638P,DANUB

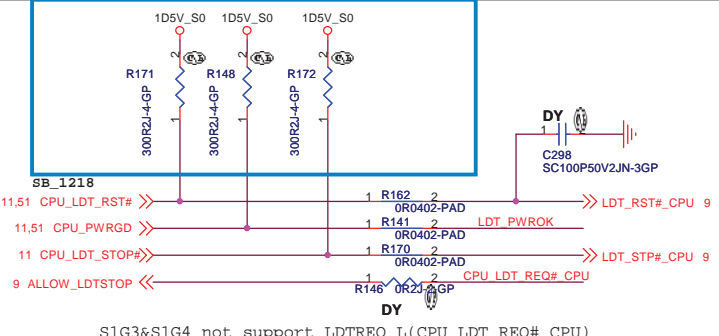
62.10055.111

ACPU1C	MEM-DATA		
MA_DATA0	MB_DATA0	C11	MEM_MB_DATA0 16
MA_DATA1	MB_DATA1	A11	MEM_MB_DATA1 16
MA_DATA2	MB_DATA2	A14	MEM_MB_DATA2 16
MA_DATA3	MB_DATA3	B14	MEM_MB_DATA3 16
MA_DATA4	MB_DATA4	G11	MEM_MB_DATA4 16
MA_DATA5	MB_DATA5	D12	MEM_MB_DATA5 16
MA_DATA6	MB_DATA6	A13	MEM_MB_DATA6 16
MA_DATA7	MB_DATA7	A15	MEM_MB_DATA7 16
MA_DATA8	MB_DATA8	A16	MEM_MB_DATA8 16
MA_DATA9	MB_DATA9	A19	MEM_MB_DATA9 16
MA_DATA10	MB_DATA10	A20	MEM_MB_DATA10 16
MA_DATA11	MB_DATA11	C14	MEM_MB_DATA11 16
MA_DATA12	MB_DATA12	D14	MEM_MB_DATA12 16
MA_DATA13	MB_DATA13	C18	MEM_MB_DATA13 16
MA_DATA14	MB_DATA14	D18	MEM_MB_DATA14 16
MA_DATA15	MB_DATA15	D20	MEM_MB_DATA15 16
MA_DATA16	MB_DATA16	A21	MEM_MB_DATA16 16
MA_DATA17	MB_DATA17	D24	MEM_MB_DATA17 16
MA_DATA18	MB_DATA18	C25	MEM_MB_DATA18 16
MA_DATA19	MB_DATA19	B20	MEM_MB_DATA19 16
MA_DATA20	MB_DATA20	C20	MEM_MB_DATA20 16
MA_DATA21	MB_DATA21	B24	MEM_MB_DATA21 16
MA_DATA22	MB_DATA22	C24	MEM_MB_DATA22 16
MA_DATA23	MB_DATA23	E23	MEM_MB_DATA23 16
MA_DATA24	MB_DATA24	C24	MEM_MB_DATA24 16
MA_DATA25	MB_DATA25	G25	MEM_MB_DATA25 16
MA_DATA26	MB_DATA26	G26	MEM_MB_DATA26 16
MA_DATA27	MB_DATA27	C26	MEM_MB_DATA27 16
MA_DATA28	MB_DATA28	D26	MEM_MB_DATA28 16
MA_DATA29	MB_DATA29	G23	MEM_MB_DATA29 16
MA_DATA30	MB_DATA30	C24	MEM_MB_DATA30 16
MA_DATA31	MB_DATA31	AA24	MEM_MB_DATA31 16
MA_DATA32	MB_DATA32	AA23	MEM_MB_DATA32 16
MA_DATA33	MB_DATA33	AD24	MEM_MB_DATA33 16
MA_DATA34	MB_DATA34	AE24	MEM_MB_DATA34 16
MA_DATA35	MB_DATA35	AA26	MEM_MB_DATA35 16
MA_DATA36	MB_DATA36	AA26	MEM_MB_DATA36 16
MA_DATA37	MB_DATA37	AA26	MEM_MB_DATA37 16
MA_DATA38	MB_DATA38	AD26	MEM_MB_DATA38 16
MA_DATA39	MB_DATA39	AC22	MEM_MB_DATA39 16
MA_DATA40	MB_DATA40	AD22	MEM_MB_DATA40 16
MA_DATA41	MB_DATA41	AE20	MEM_MB_DATA41 16
MA_DATA42	MB_DATA42	AF20	MEM_MB_DATA42 16
MA_DATA43	MB_DATA43	AE24	MEM_MB_DATA43 16
MA_DATA44	MB_DATA44	AE23	MEM_MB_DATA44 16
MA_DATA45	MB_DATA45	AC20	MEM_MB_DATA45 16
MA_DATA46	MB_DATA46	AD20	MEM_MB_DATA46 16
MA_DATA47	MB_DATA47	AD18	MEM_MB_DATA47 16
MA_DATA48	MB_DATA48	AE18	MEM_MB_DATA48 16
MA_DATA49	MB_DATA49	AC14	MEM_MB_DATA49 16
MA_DATA50	MB_DATA50	AD14	MEM_MB_DATA50 16
MA_DATA51	MB_DATA51	AE19	MEM_MB_DATA51 16
MA_DATA52	MB_DATA52	AC18	MEM_MB_DATA52 16
MA_DATA53	MB_DATA53	AE16	MEM_MB_DATA53 16
MA_DATA54	MB_DATA54	AE15	MEM_MB_DATA54 16
MA_DATA55	MB_DATA55	AE13	MEM_MB_DATA55 16
MA_DATA56	MB_DATA56	AC12	MEM_MB_DATA56 16
MA_DATA57	MB_DATA57	AE11	MEM_MB_DATA57 16
MA_DATA58	MB_DATA58	Y11	MEM_MB_DATA58 16
MA_DATA59	MB_DATA59	AE14	MEM_MB_DATA59 16
MA_DATA60	MB_DATA60	AE14	MEM_MB_DATA60 16
MA_DATA61	MB_DATA61	AE11	MEM_MB_DATA61 16
MA_DATA62	MB_DATA62	AD11	MEM_MB_DATA62 16
MA_DATA63	MB_DATA63		MEM_MB_DATA63 16
MA_DM0	MB_DM0	A12	MEM_MB_DM0 16
MA_DM1	MB_DM1	B16	MEM_MB_DM1 16
MA_DM2	MB_DM2	A22	MEM_MB_DM2 16
MA_DM3	MB_DM3	E25	MEM_MB_DM3 16
MA_DM4	MB_DM4	AE26	MEM_MB_DM4 16
MA_DM5	MB_DM5	AC16	MEM_MB_DM5 16
MA_DM6	MB_DM6	AD12	MEM_MB_DM6 16
MA_DM7	MB_DM7		MEM_MB_DM7 16
MA_DQS_H0	MB_DQS_H0	C12	MEM_MB_DQS0_P 16
MA_DQS_L0	MB_DQS_L0	B12	MEM_MB_DQS0_N 16
MA_DQS_H1	MB_DQS_H1	D12	MEM_MB_DQS1_P 16
MA_DQS_L1	MB_DQS_L1	C16	MEM_MB_DQS1_N 16
MA_DQS_H2	MB_DQS_H2	A24	MEM_MB_DQS2_P 16
MA_DQS_L2	MB_DQS_L2	AE22	MEM_MB_DQS2_N 16
MA_DQS_H3	MB_DQS_H3	F26	MEM_MB_DQS3_P 16
MA_DQS_L3	MB_DQS_L3	E26	MEM_MB_DQS3_N 16
MA_DQS_H4	MB_DQS_H4	AC25	MEM_MB_DQS4_P 16
MA_DQS_L4	MB_DQS_L4	AC26	MEM_MB_DQS4_N 16
MA_DQS_H5	MB_DQS_H5	AE21	MEM_MB_DQS5_P 16
MA_DQS_L5	MB_DQS_L5	AE22	MEM_MB_DQS5_N 16
MA_DQS_H6	MB_DQS_H6	AE16	MEM_MB_DQS6_P 16
MA_DQS_L6	MB_DQS_L6	AD16	MEM_MB_DQS6_N 16
MA_DQS_H7	MB_DQS_H7	AE12	MEM_MB_DQS7_P 16
MA_DQS_L7	MB_DQS_L7	AE12	MEM_MB_DQS7_N 16

JE70-DN

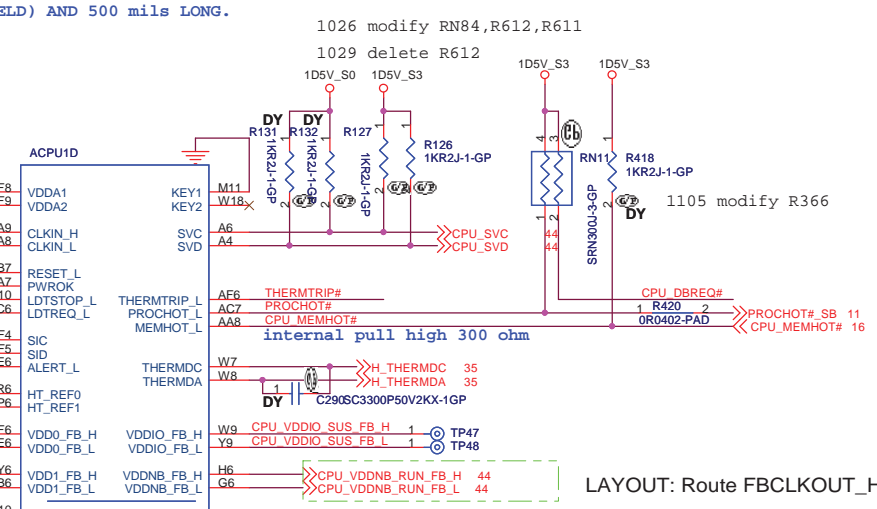
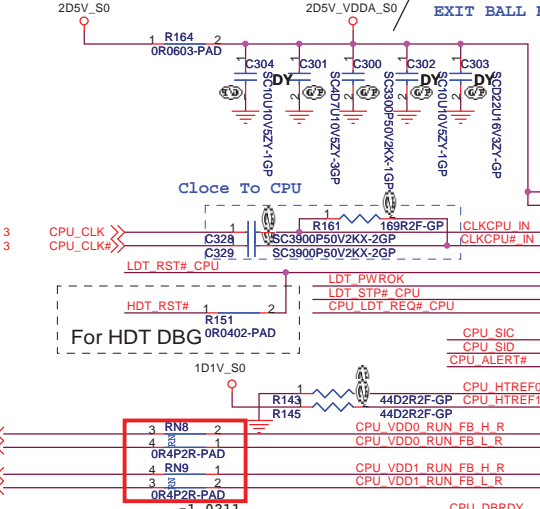
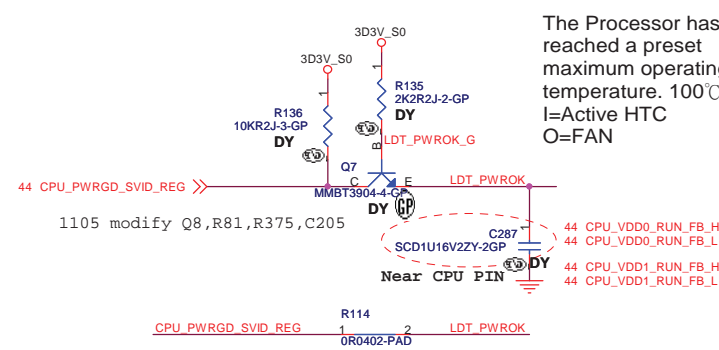
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU DDR (2/4)		
Size	Document Number	Rev
A3	JE70-DN	SB
Date:	Monday, March 01, 2010	Sheet 5 of 63

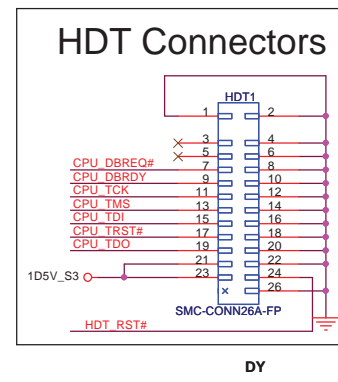
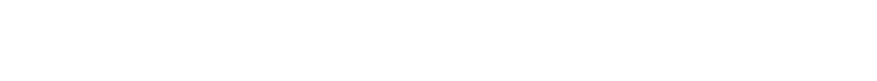
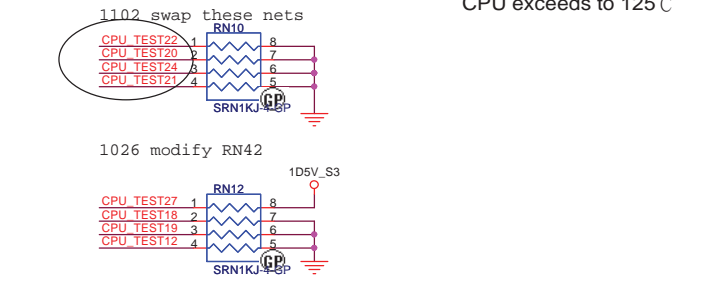
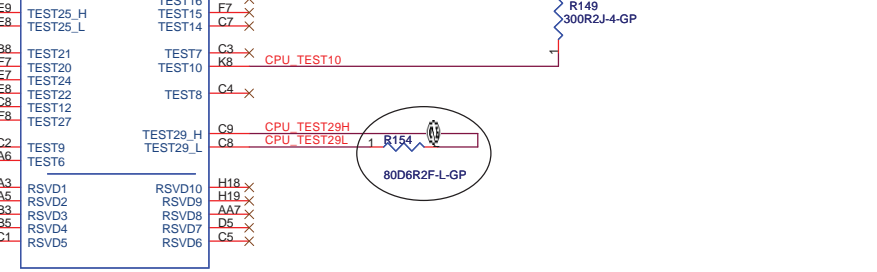
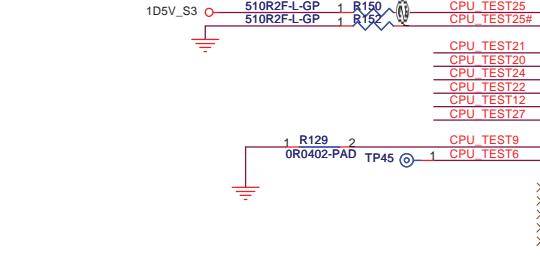
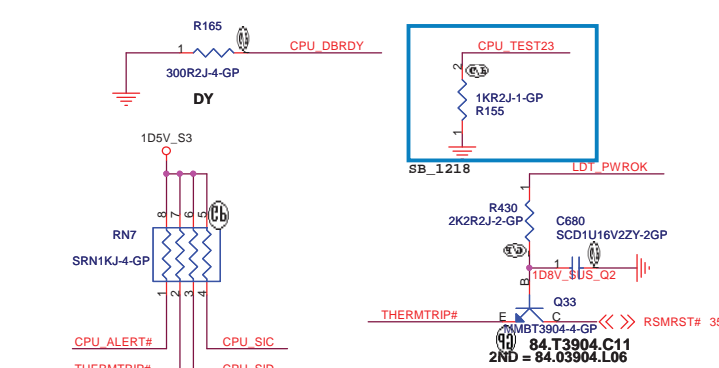
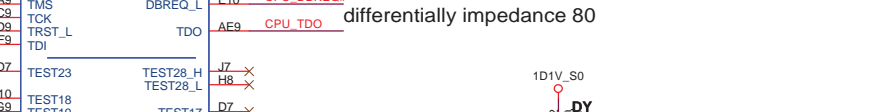


IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



1105 modify Q8,R81,R375,C205



JE70-DN

緯創資通 Wistron Corporation

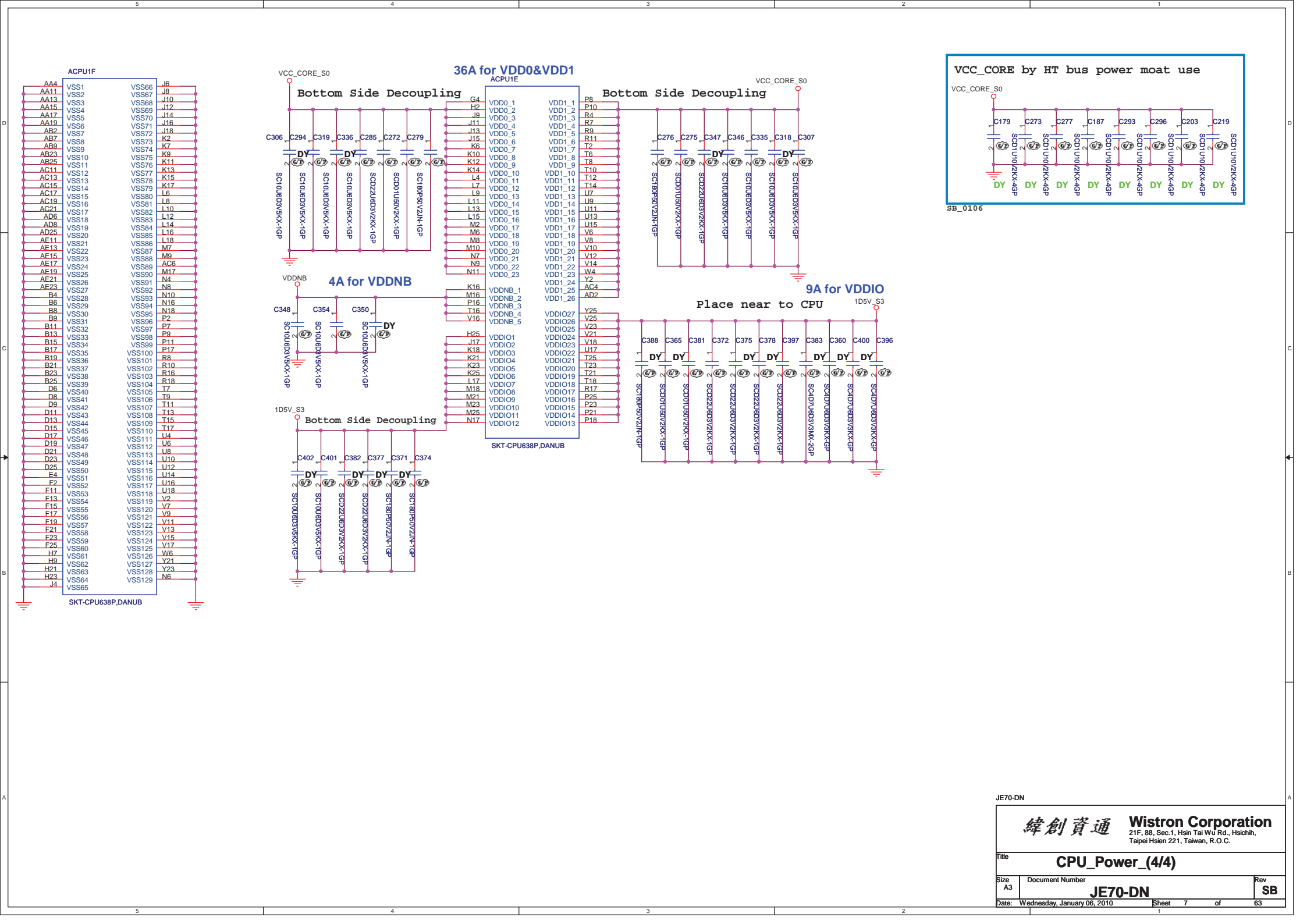
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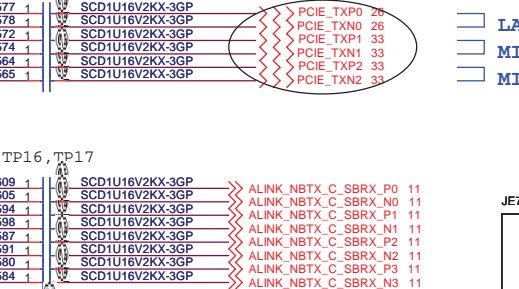
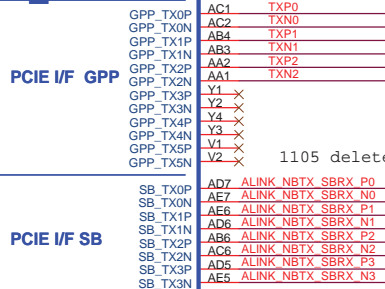
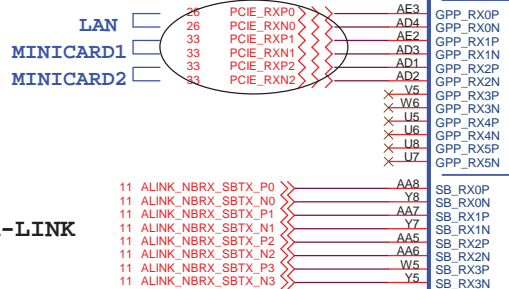
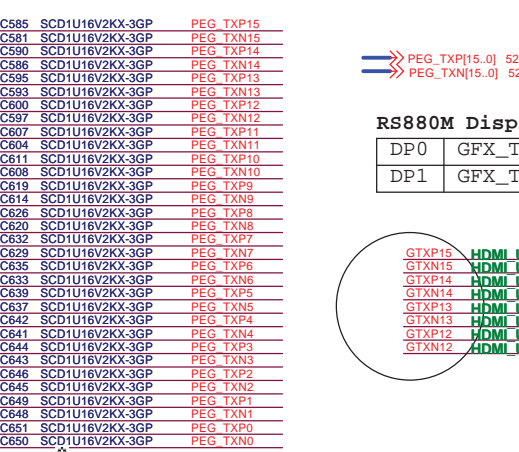
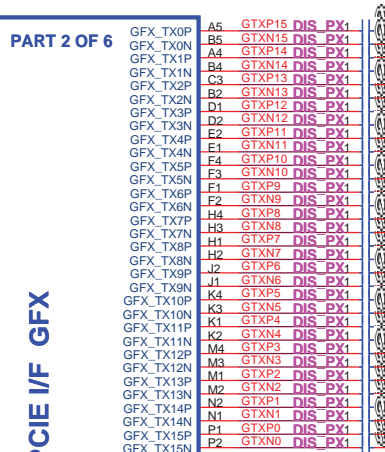
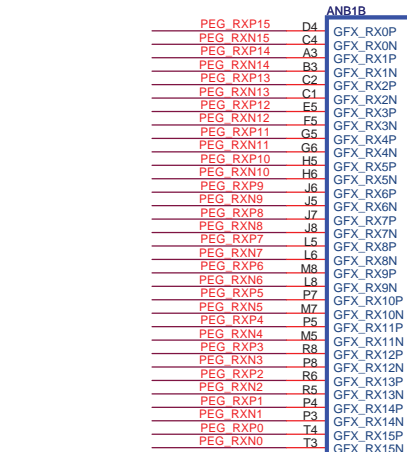
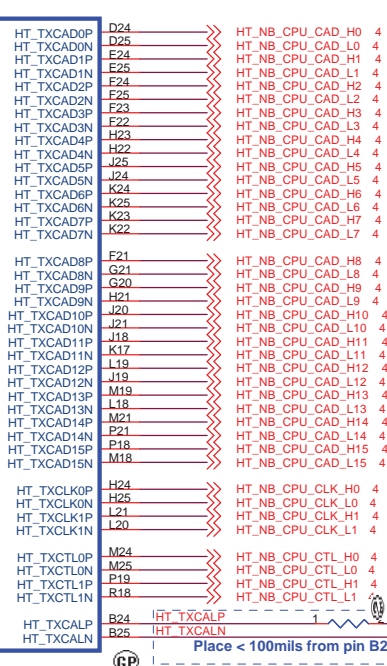
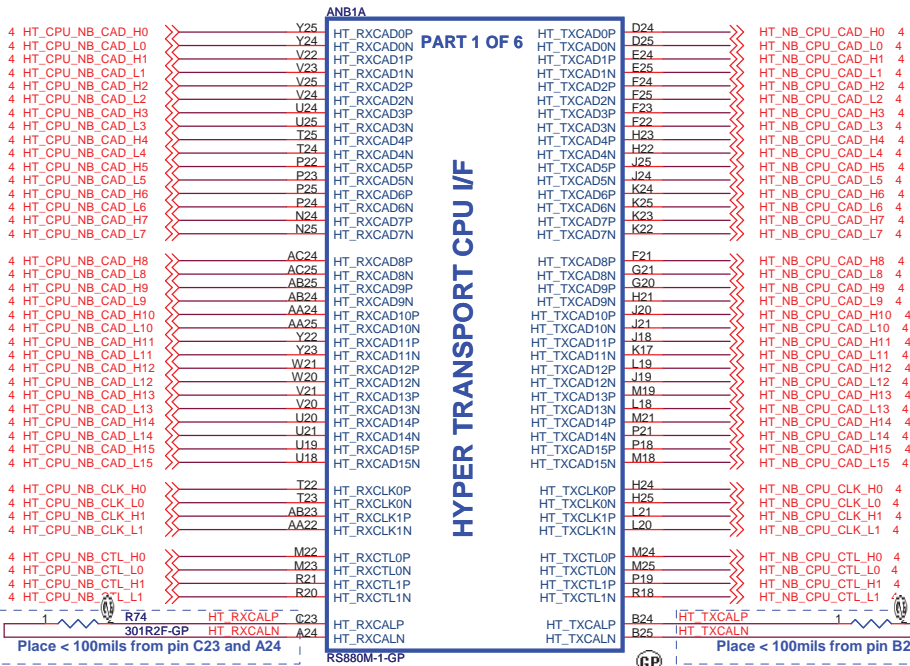
Title CPU_Control&Debug_(3/4)

Size A3 Document Number JE70-DN

Date: Tuesday, February 23, 2010 Sheet 6 of 63

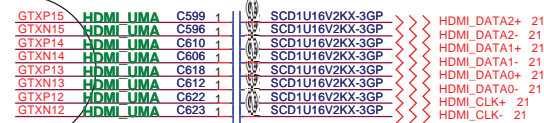
Rev SB





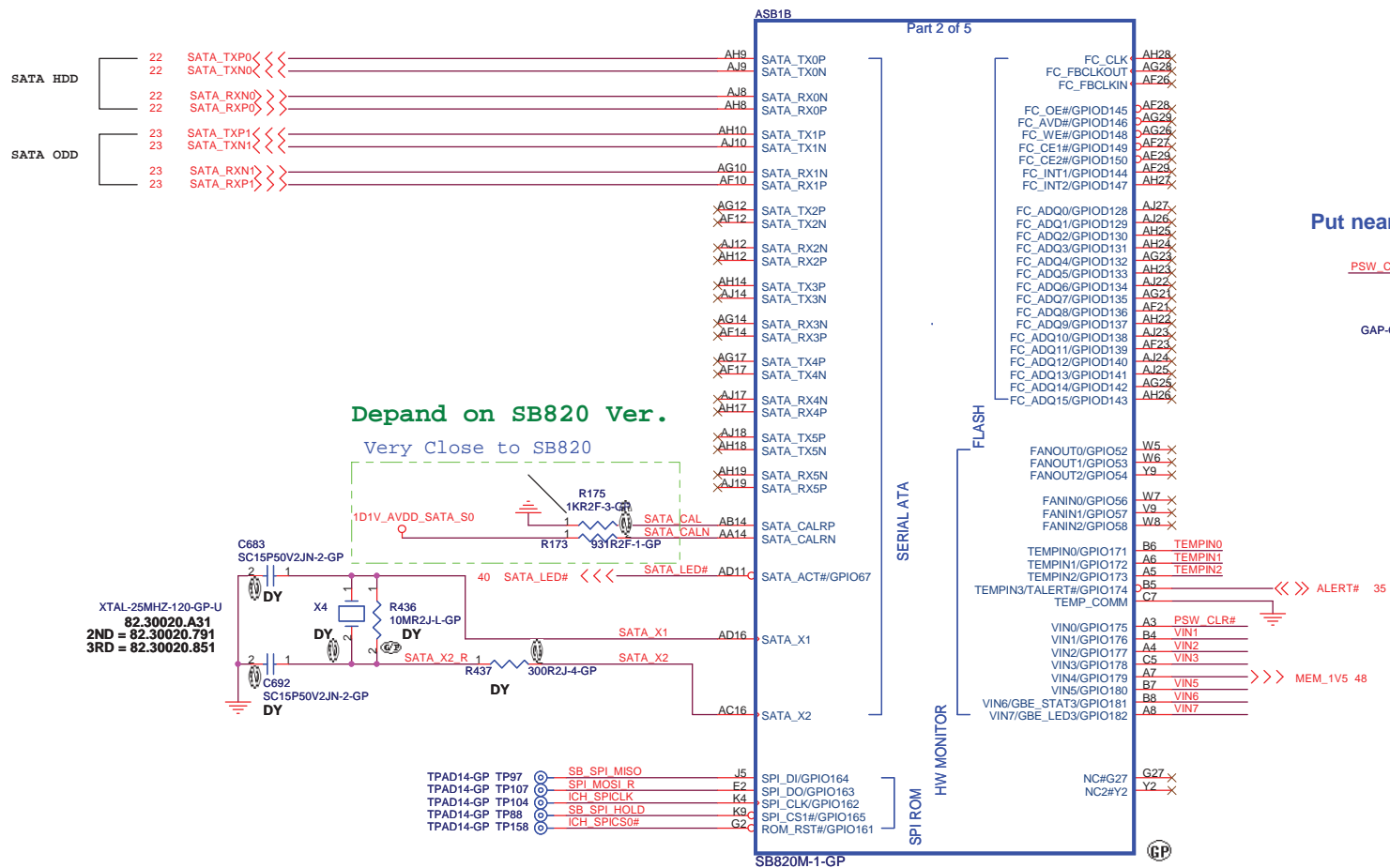
RS880M Display Port Support(muxed on GFX)

DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1







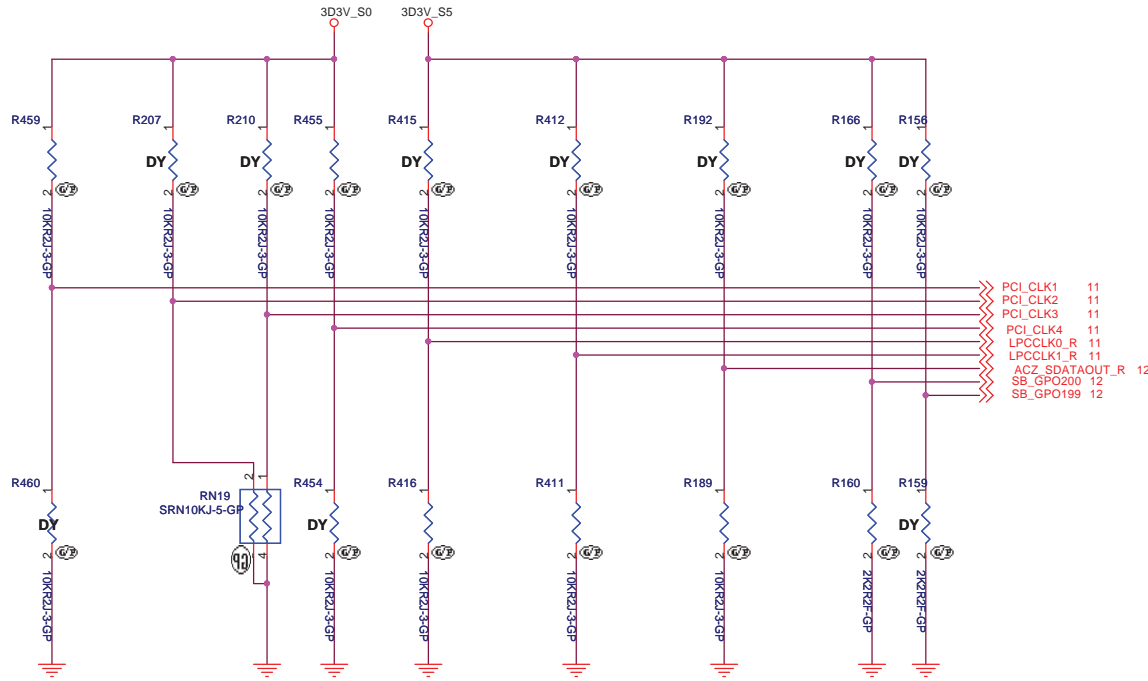


JE70-DN

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ATI-SB820 SATA-IDE (3/5)			
Size	Document Number	Rev	SB
A3	JE70-DN		
Date:	Tuesday, February 23, 2010	Sheet	13 of 63

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



1118 modify R412,R411

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP DEFAULT	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

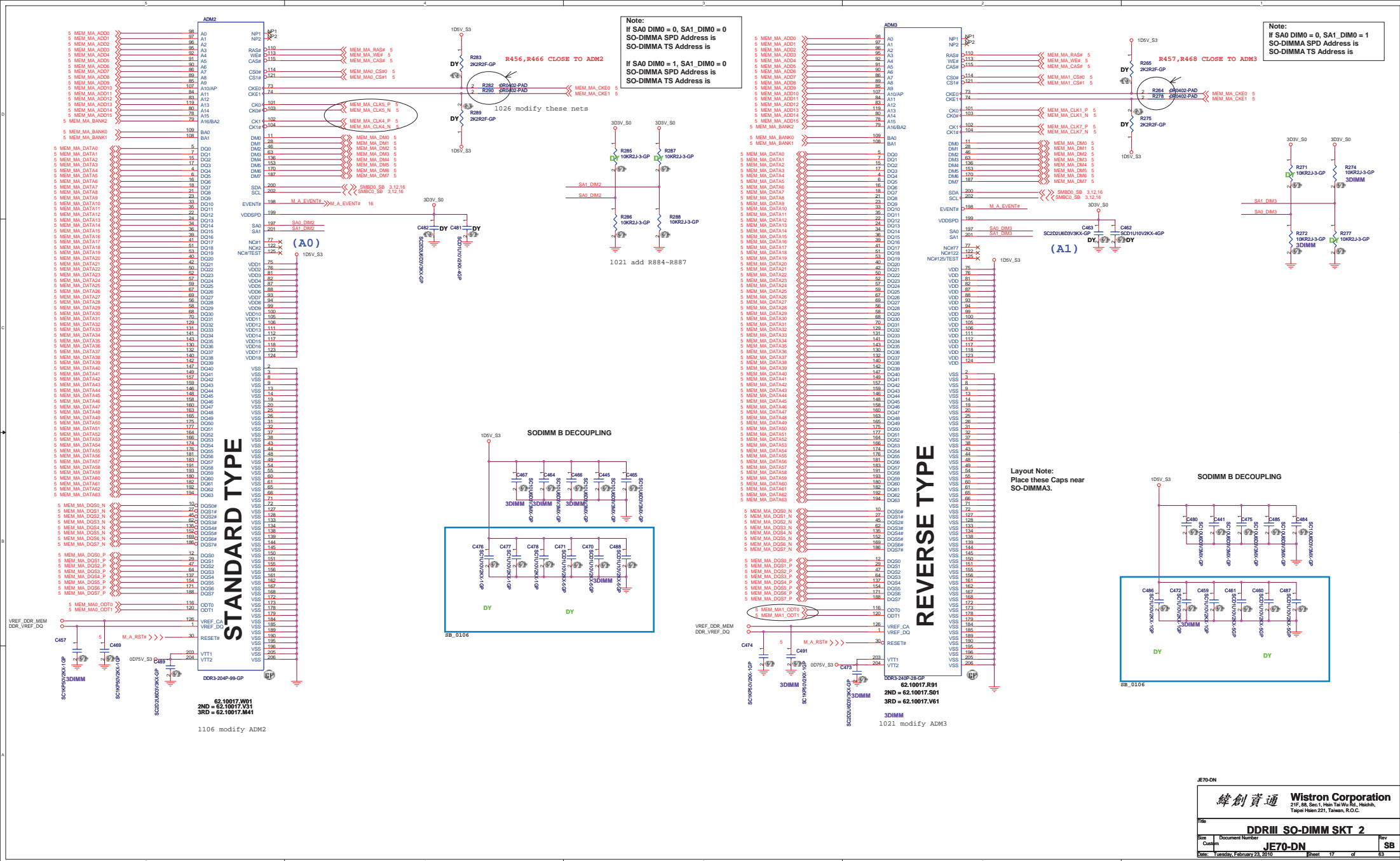
TPAD14-GP	TP89	PCI_AD23	11
TPAD14-GP	TP87	PCI_AD24	11
TPAD14-GP	TP85	PCI_AD25	11
TPAD14-GP	TP93	PCI_AD26	11
TPAD14-GP	TP98	PCI_AD27	11
TPAD14-GP	TP156	PCI_AD28	11
TPAD14-GP	TP159	PCI_AD29	11
TPAD14-GP	TP154	PCI_AD30	11

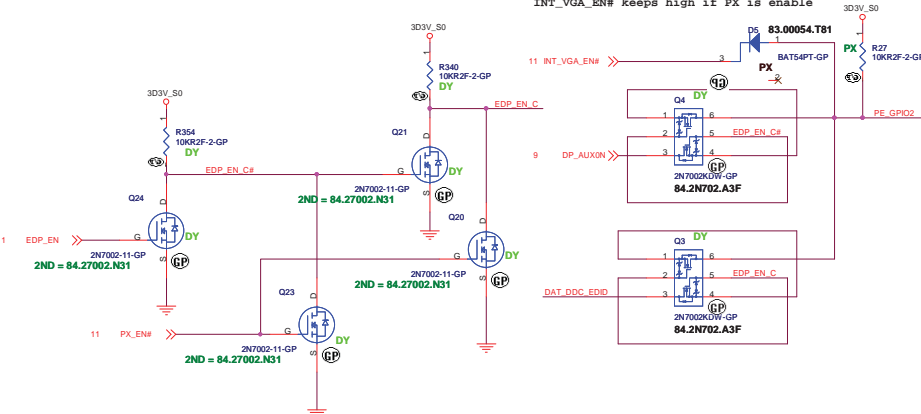
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

JE70-DN

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
ATI-SB820 STRAPPING (5/5)	
Size	Document Number
A3	JE70-DN
Date: Tuesday, February 23, 2010	Rev SB
Sheet 15 of 63	





DISPLAY SUPPORT TABLE

	PX_EN#	DP_AUX0N EDP disabled	I2C_DATA EDP disabled	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	1	X	X	0	IGP (LVDS, EDP, VGA, DP)
MXM only mode	1	X	X	1	MXM (LVDS, EDP, VGA, DP)
Power Express(muxed)	0	0/1	0/1	1	MXM / IGP (LVDS, EDP, VGA); MXM (DP)
Power Express(muxless)	0	X	X	0	IGP (LVDS, EDP, VGA, DP)

PX mode display device auto detection method:
VGA: I2C interface to NB
DP: HPD

LVDS

Function	SEL
An to nB1	L
An to nB2	H

CRT

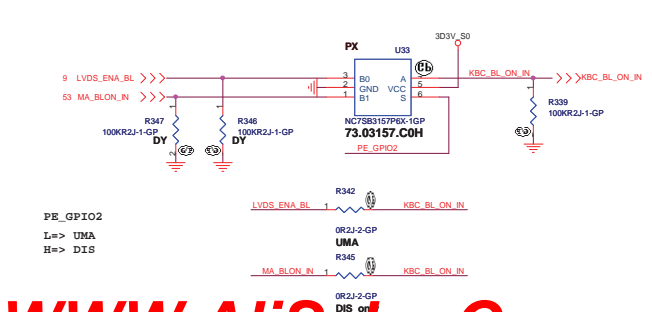
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S=0
L	H	IA1	IB1	IC1	ID1	S=1

EDID

Function Table

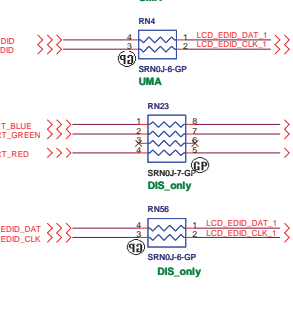
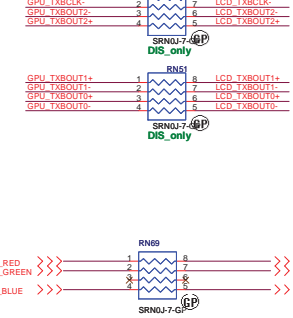
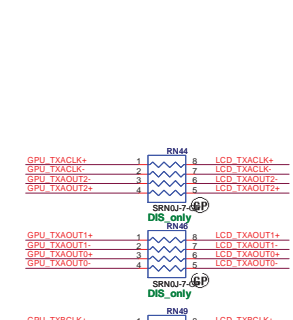
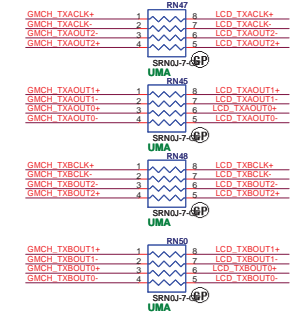
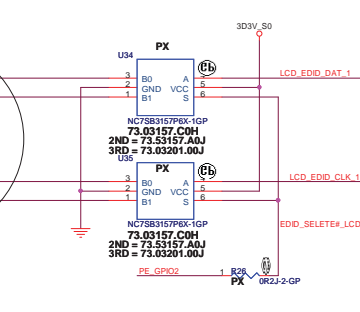
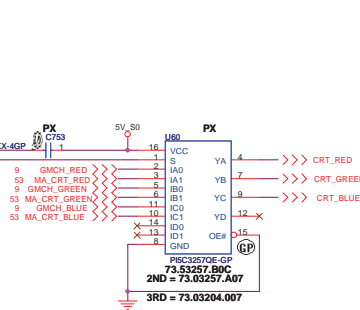
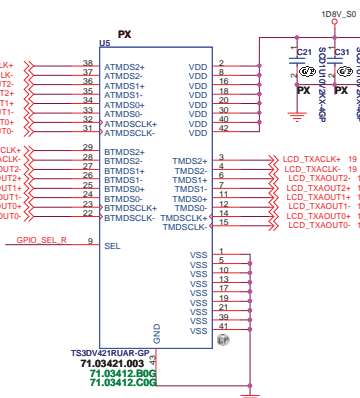
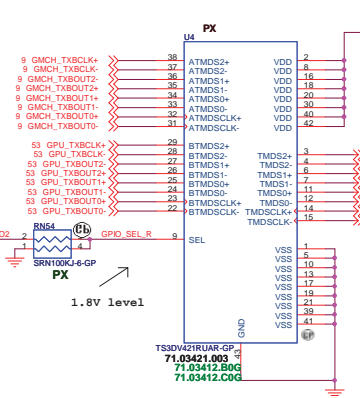
Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H= HIGH Logic Level L= LOW Logic Level



PE_GPIO2

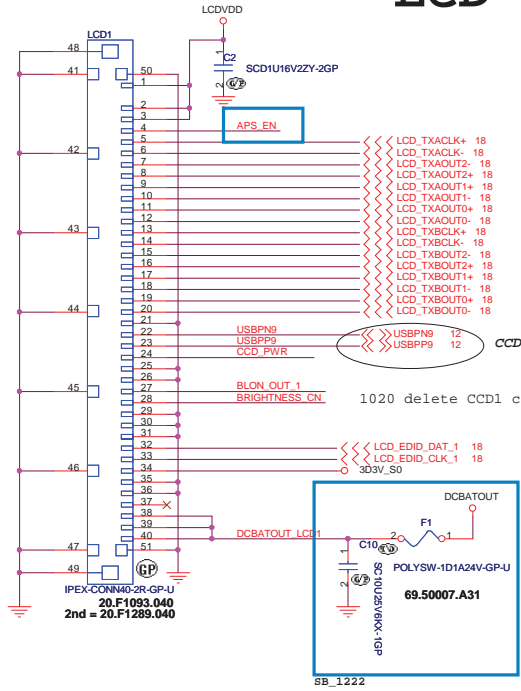
L=> UMA
H=> DIS



LCD CONN

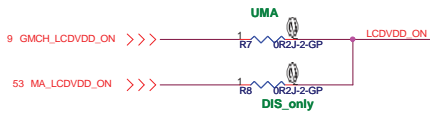
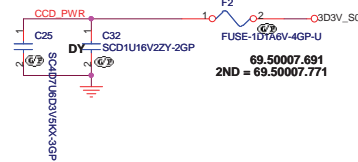
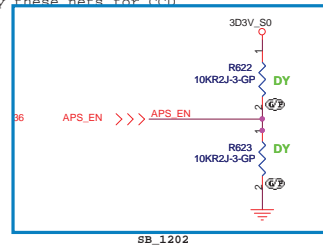
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

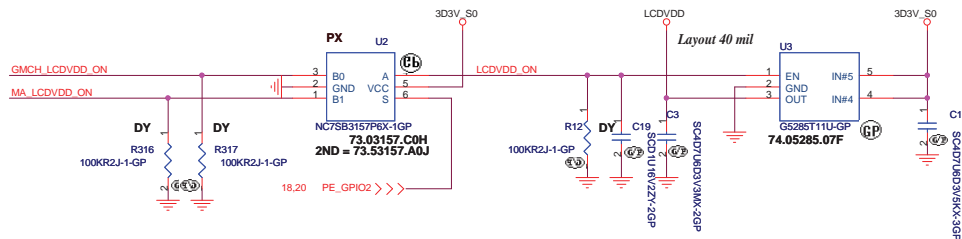


1029 add EC99,EC100

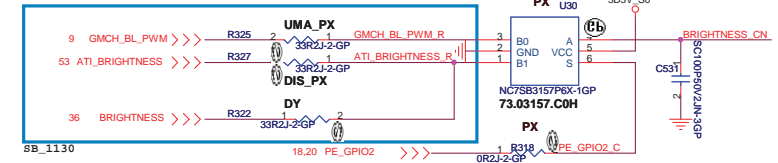
1020 delete CCD1 conn and modify these nets for CCD



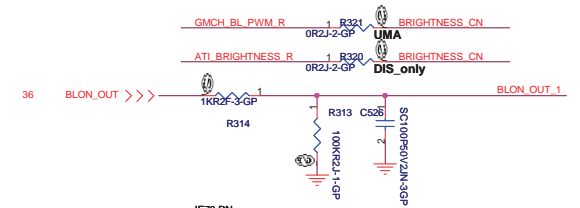
PE_GPIO2
L=> UMA
H=> DIS



Reserve direct connector to KBC



PE_GPIO2
L=> UMA
H=> DIS

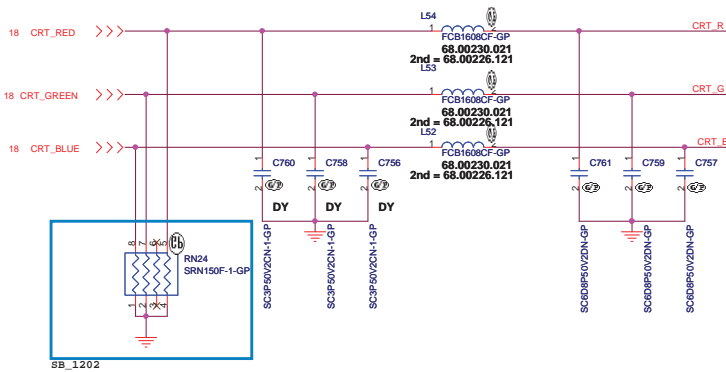


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Title	
LCD CONN	
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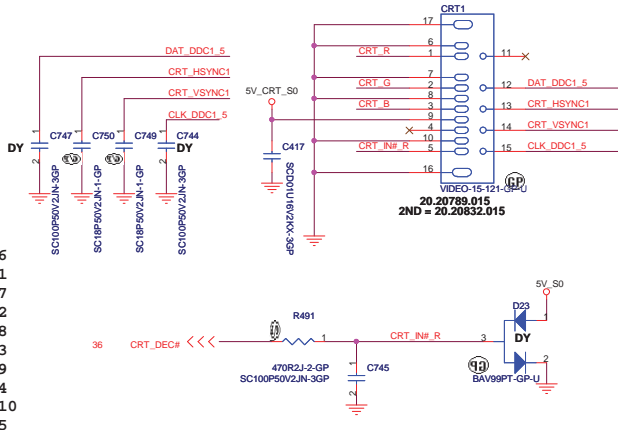
Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz



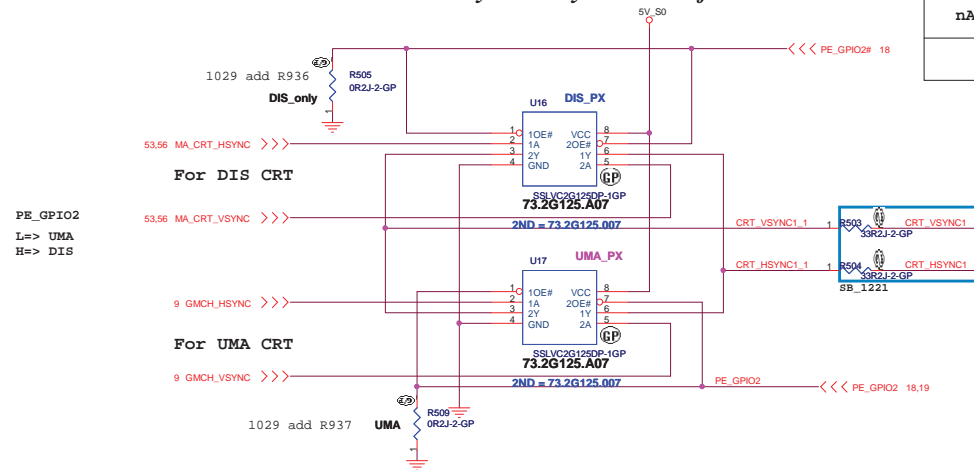
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

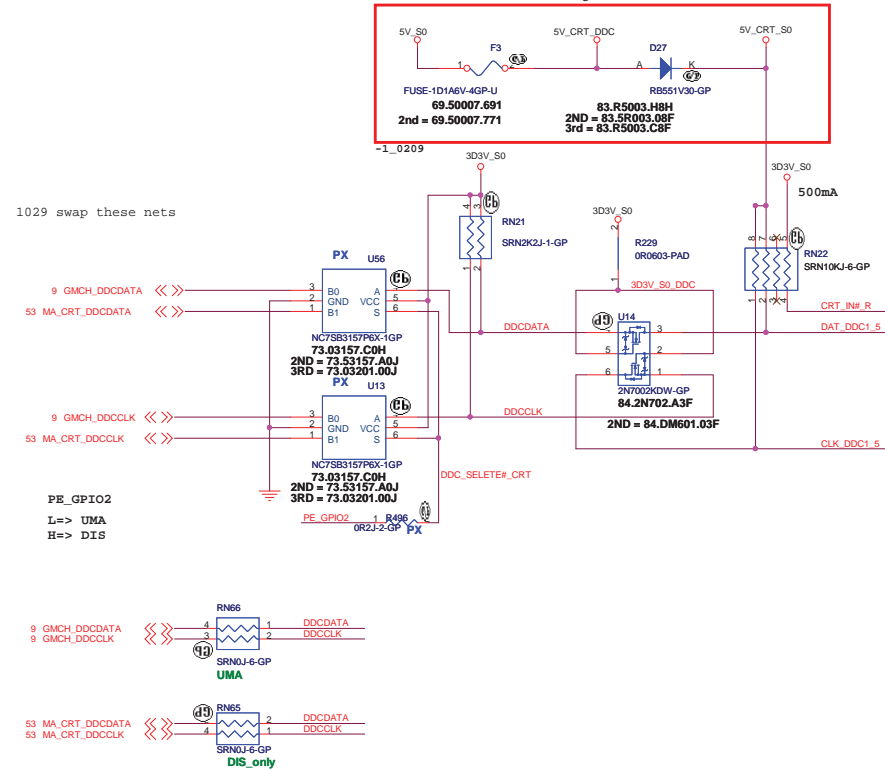


Hsync & Vsync level shift

Function	OE#
nA to nY	L
X	H



DDC_CLK & DATA level shift

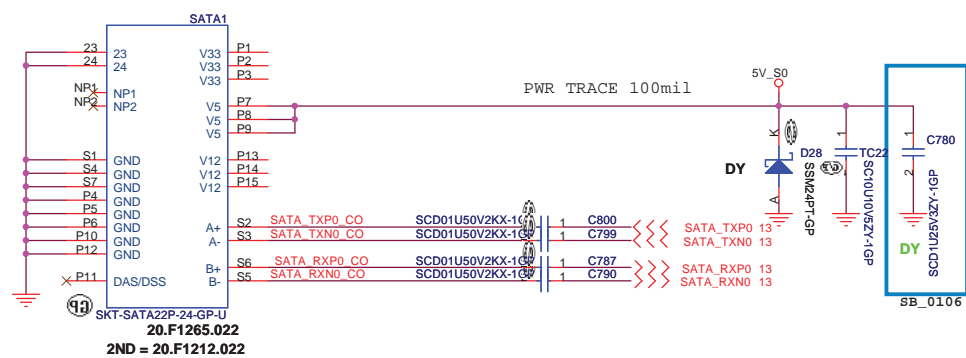


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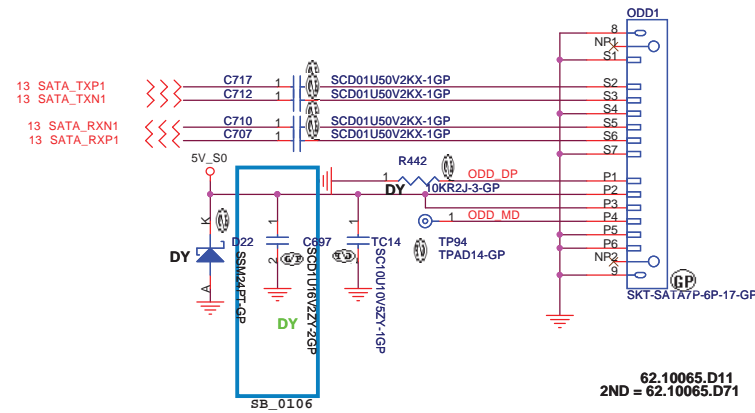
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size Document Number	
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CRT Connector		Rev
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SATA Connector



ODD Connector



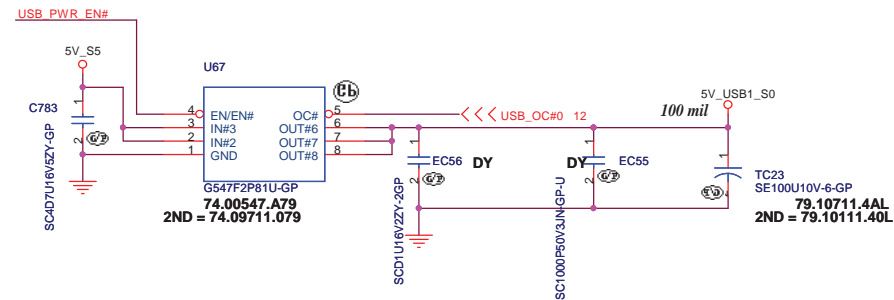
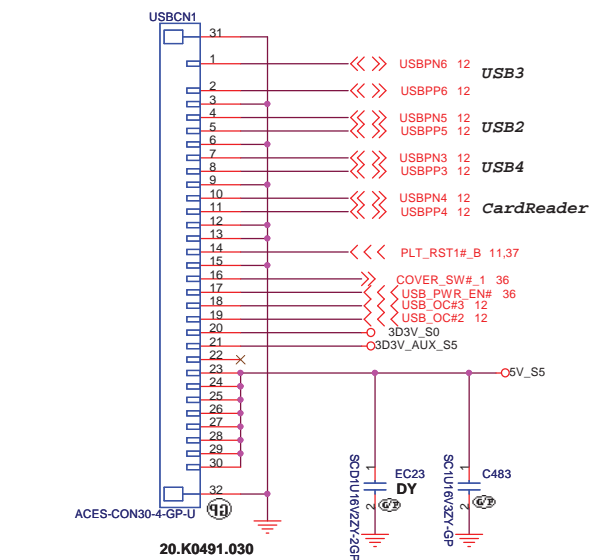
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ODD			
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1.5A / High Active Voltage 2V



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BLUETOOTH			
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USB

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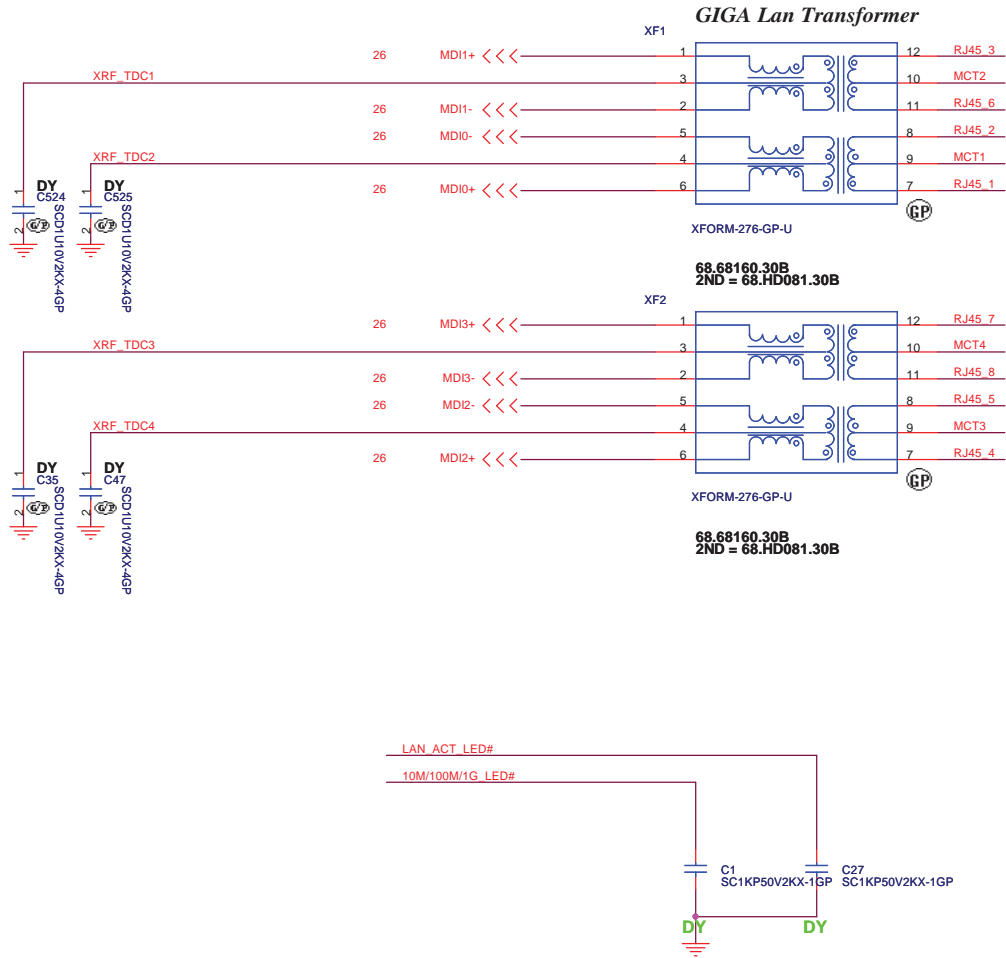
Date: Tuesday, February 23, 2010

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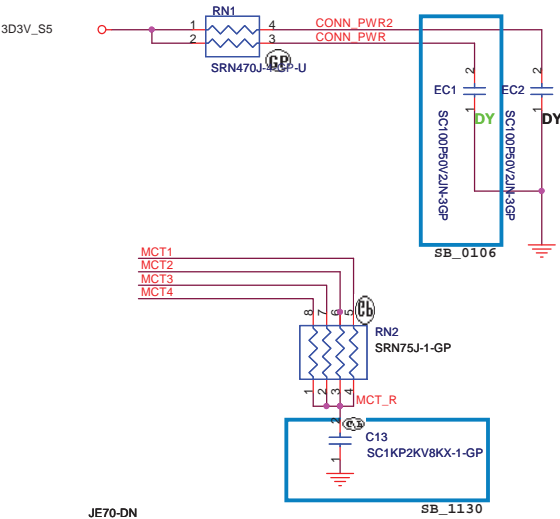
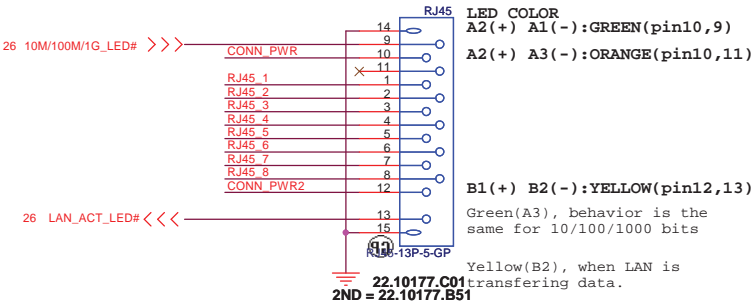
Rev	2
-----	---

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

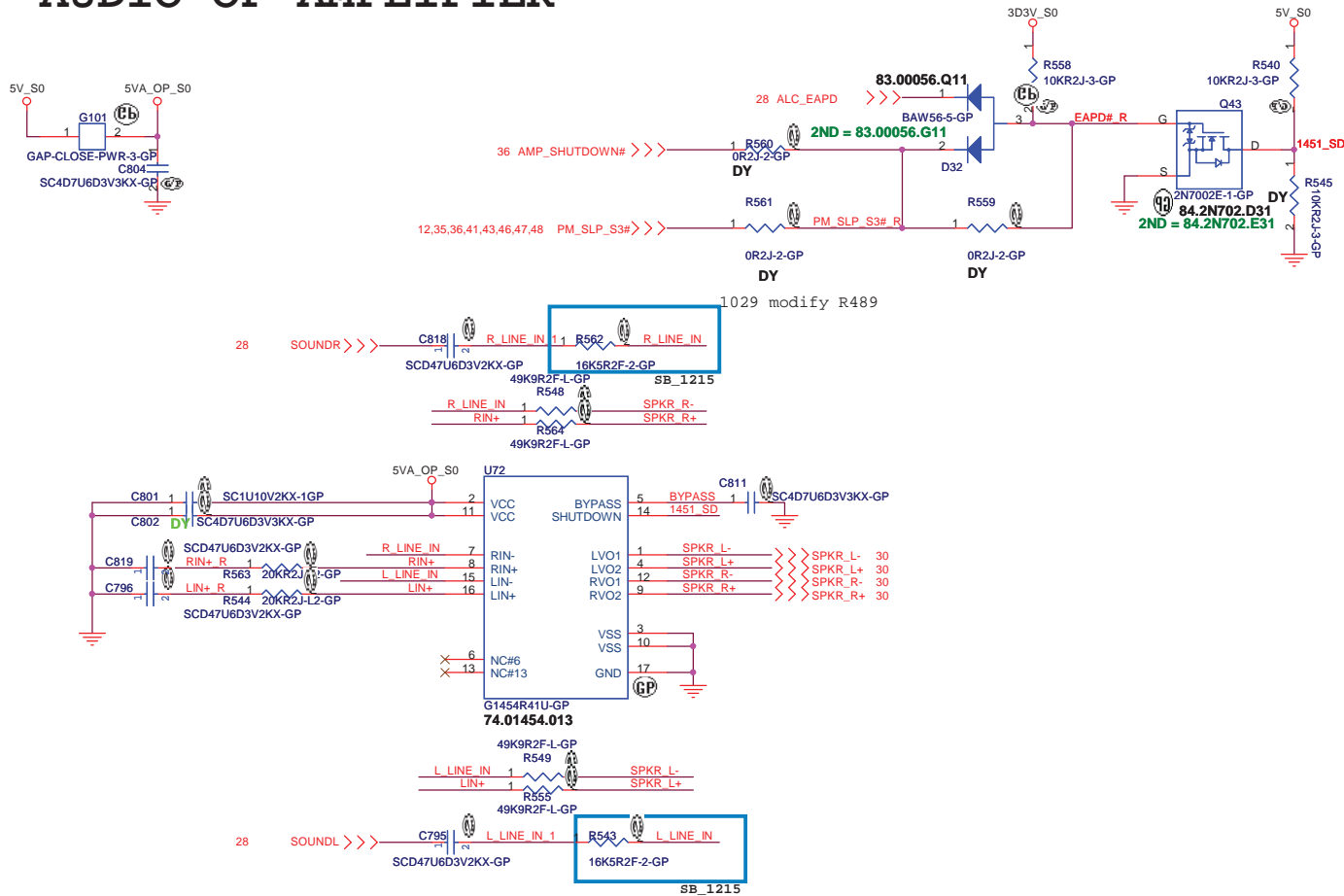
LAN Connector



LAN Connector



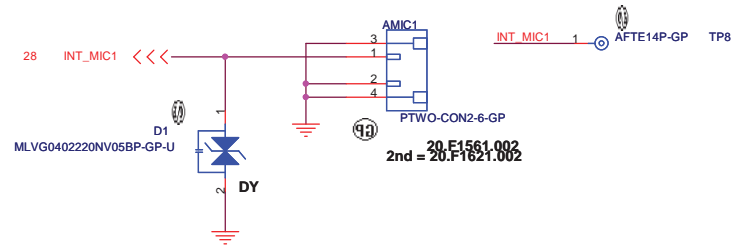
AUDIO OP AMPLIFIER



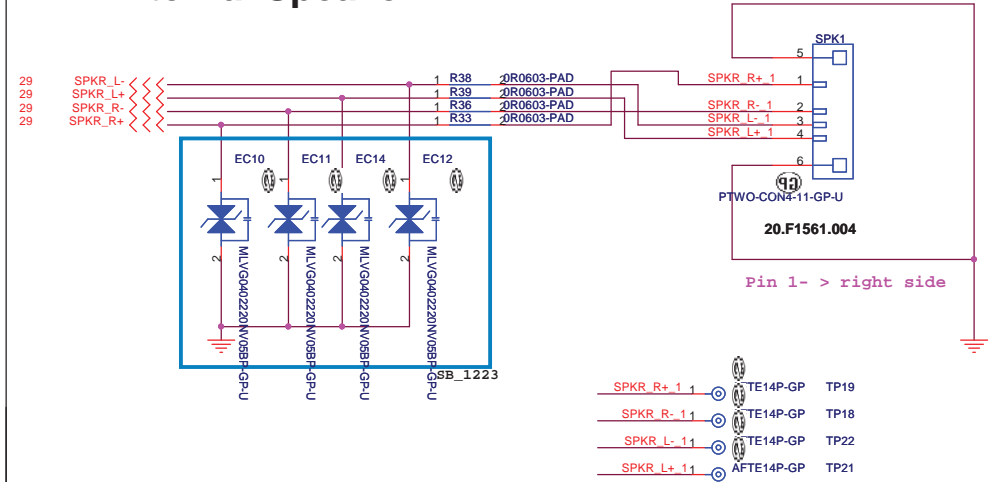
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Title: AUDIO AMP			
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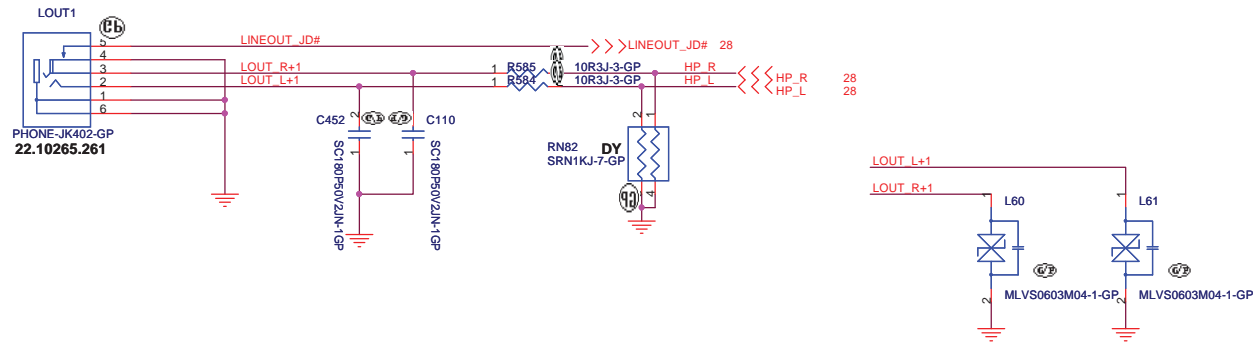
Internal Mic



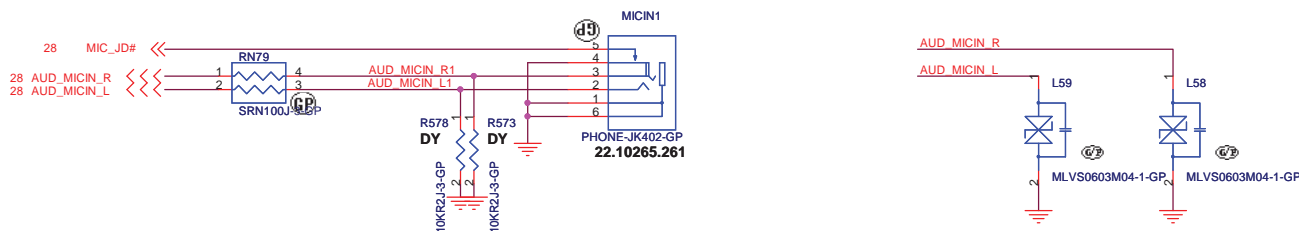
Internal Speaker



LINE OUT



MIC IN



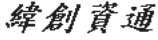
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No Modem Function

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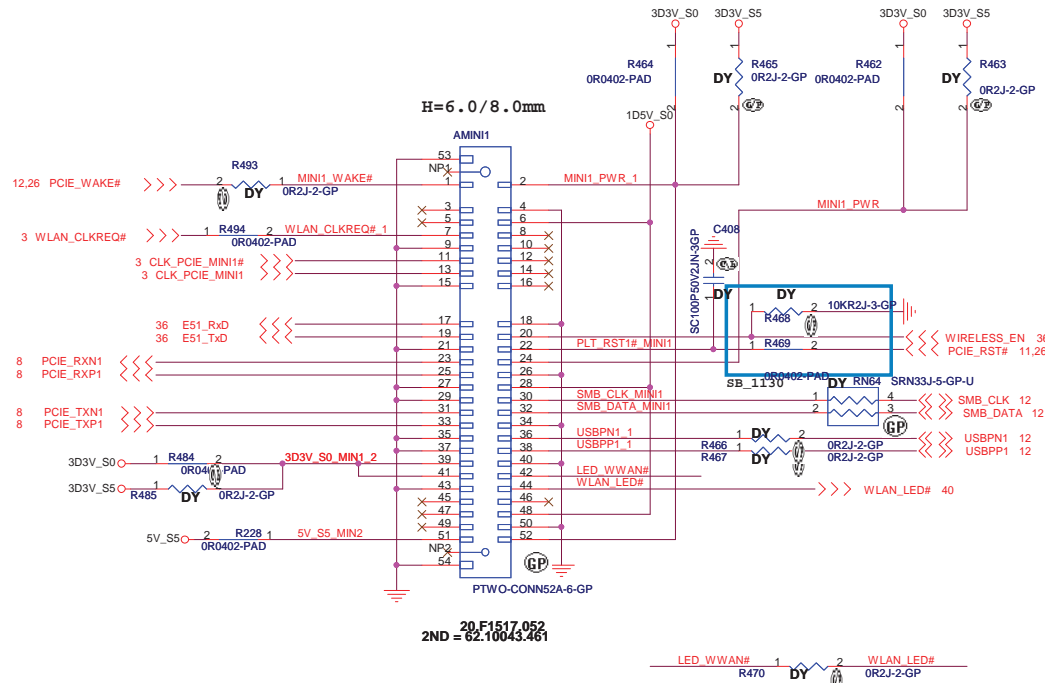
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Title			
MDC			
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5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD) on USB board

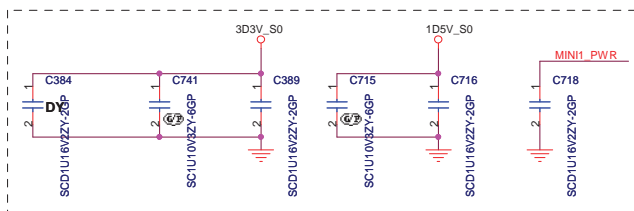
JE70-DN

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CARDREADER			
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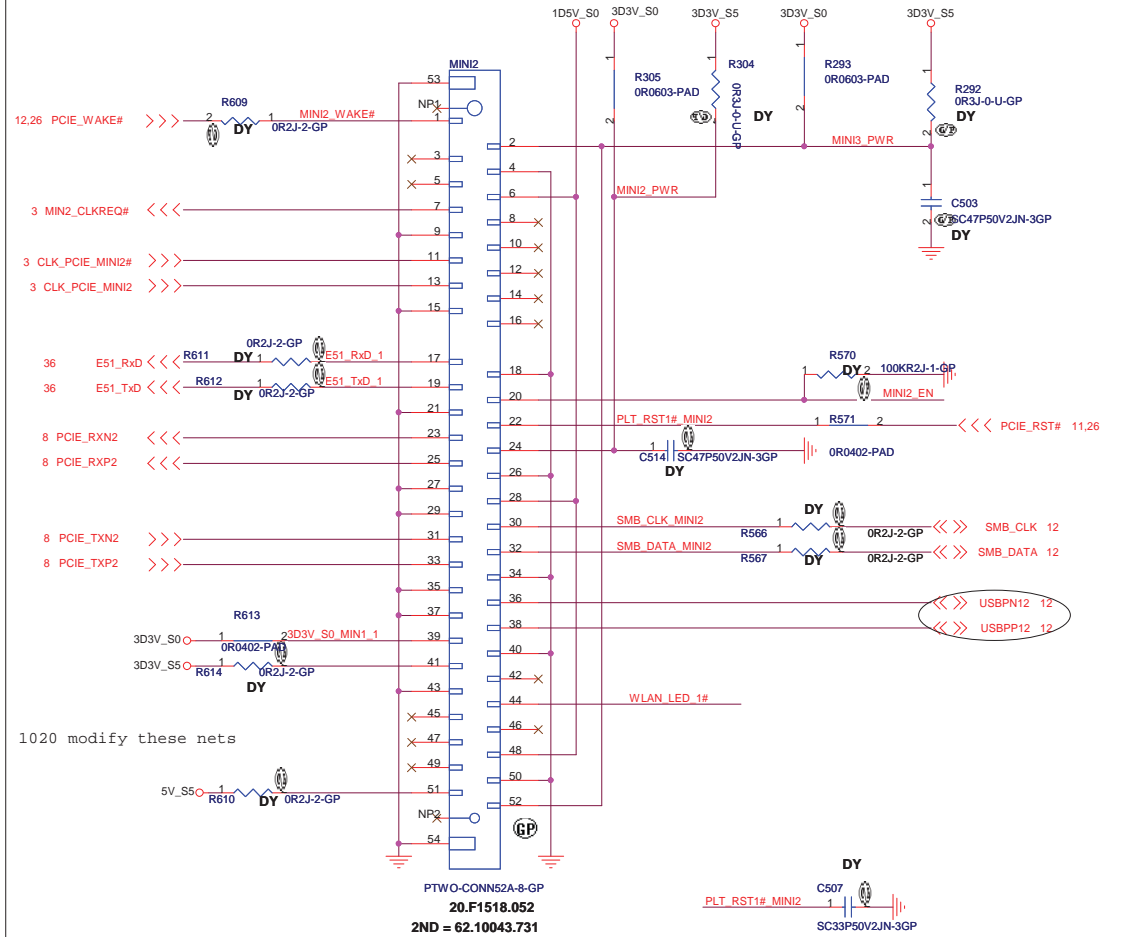
Mini Card Connector(WLAN)



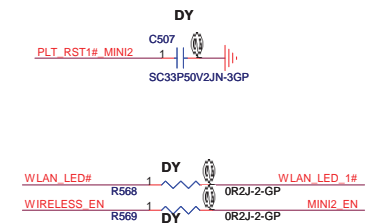
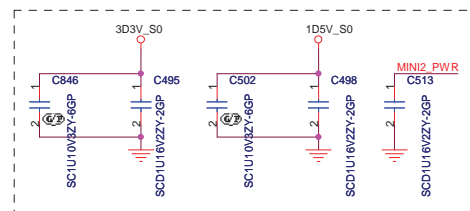
Place near AMINI1



Mini Card Function



Place near MINIC2



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	Title
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MINI CARD

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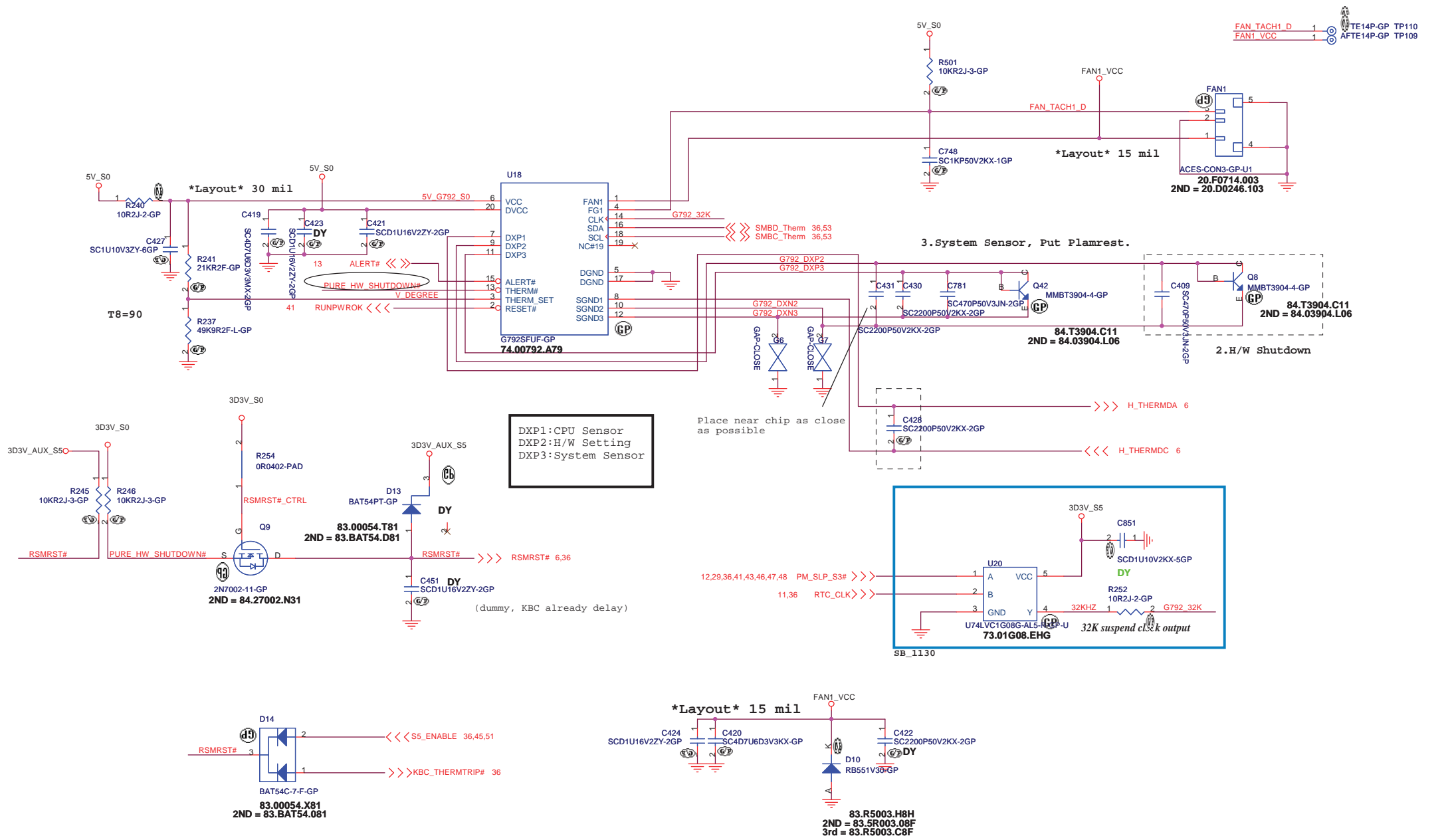
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	F
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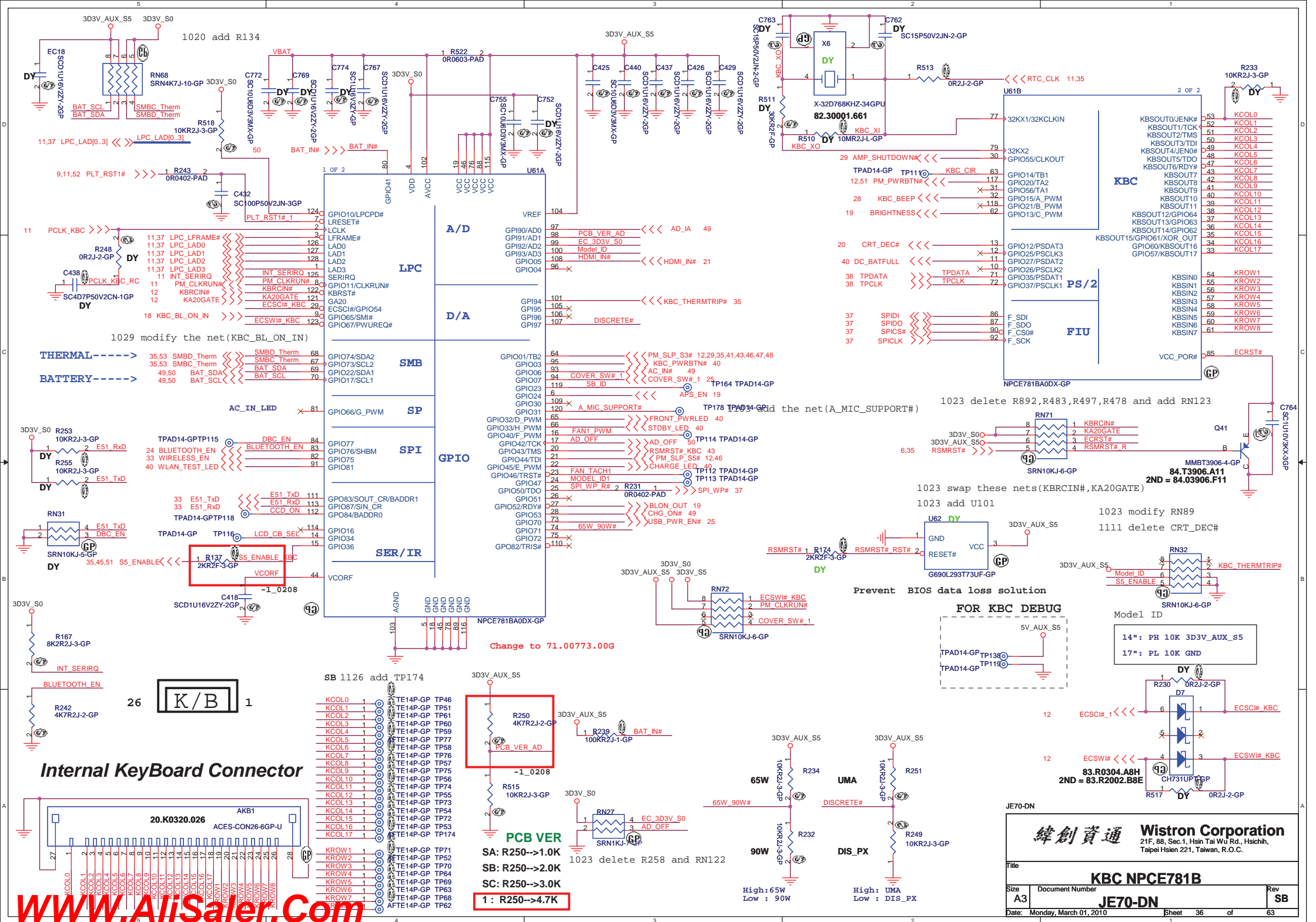
No NEWCARD Function

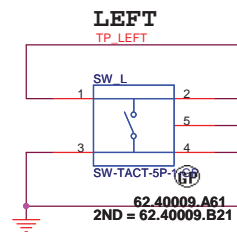
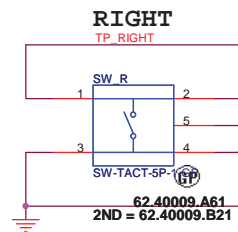
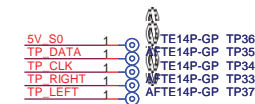
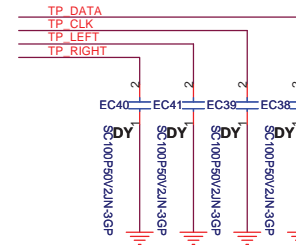
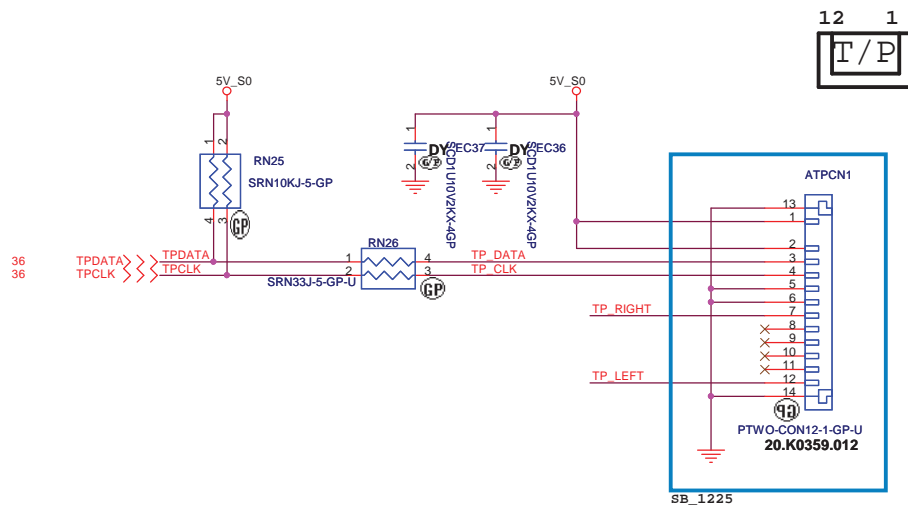
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Title			
NEW CARD			
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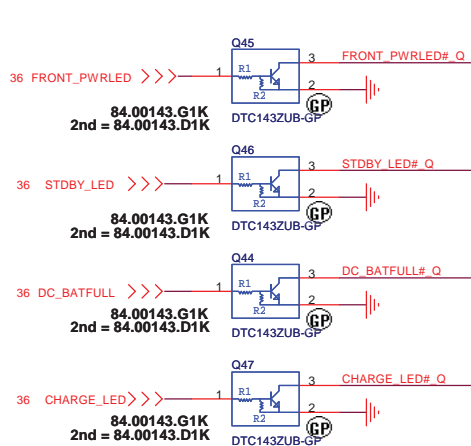
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Title		Touch PAD	
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NONE BOARD

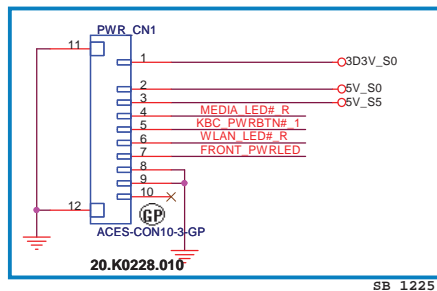
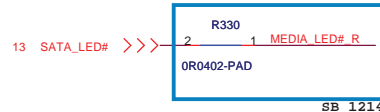
緯創資通		Wistron Corporation	
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Title			
NONE BOARD			
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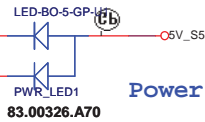
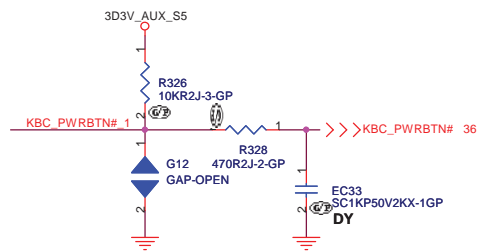
LED

FRONT_PWRLED# Q 1 R604
STDBY_LED# Q 1 R618
DC_BATFULL# Q 1 R605
CHARGE_LED# Q 1 R617

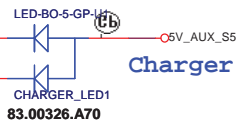
FRONT_PWRLED# Q 1 DY EC58
STDBY_LED# Q 1 DY EC61
DC_BATFULL# Q 1 DY EC57
CHARGE_LED# Q 1 DY EC60



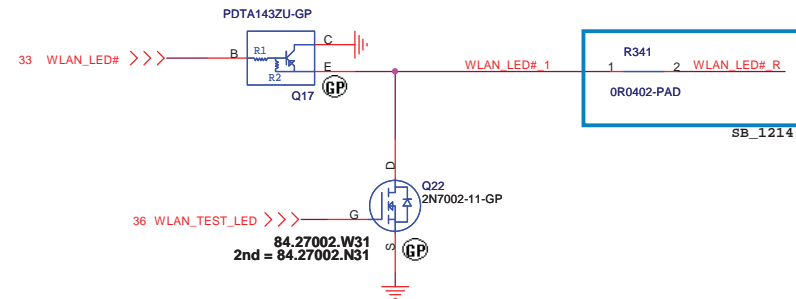
TP11 AFTE14P-G 1 3D3V_S0
TP12 AFTE14P-G 1 5V_S0
TP10 AFTE14P-G 1 5V_S5
TP13 AFTE14P-G 1 MEDIA_LED# R
TP14 AFTE14P-G 1 KBC_PWRBTN# 1
TP15 AFTE14P-G 1 WLAN_LED# R
TP16 AFTE14P-G 1 FRONT_PWRLED



Power LED

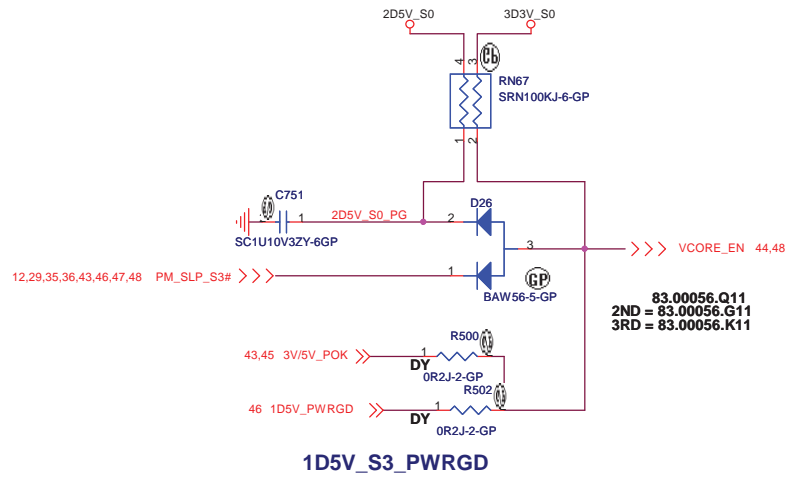


Charger LED

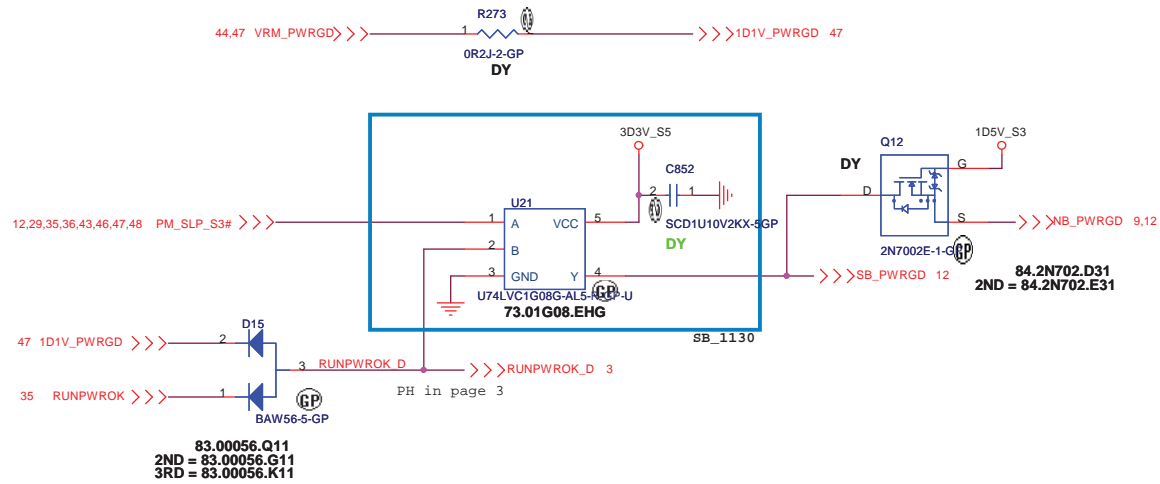


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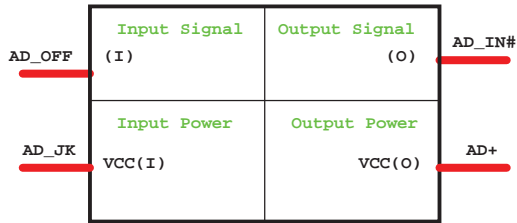


P/H @ 1D8V_S3 PAGE

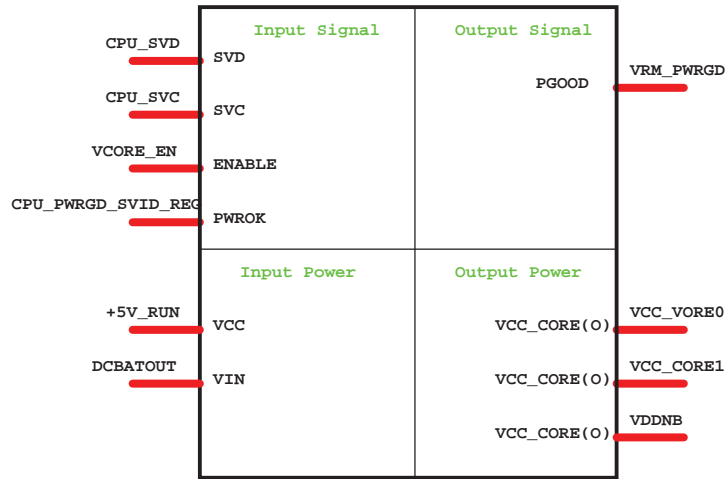


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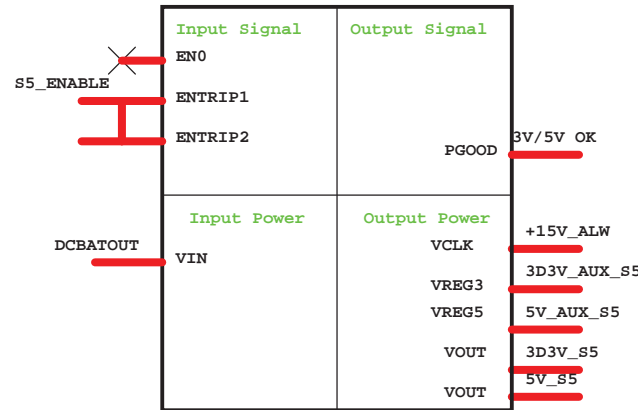
Adapter



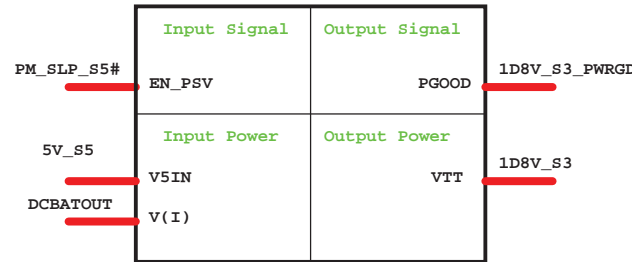
CPU_CORE ISL6265HRTZ



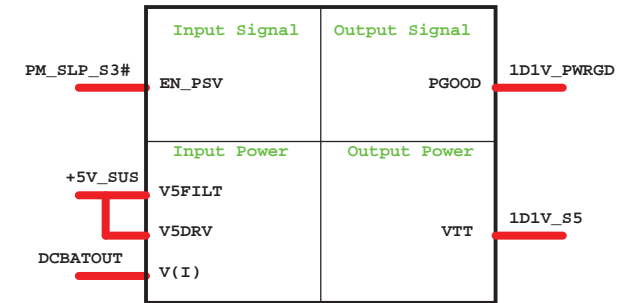
DCDC 5V/3D3V(RT8205A)



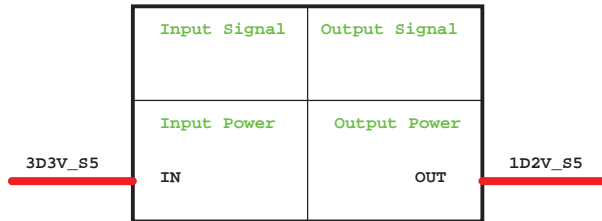
DCDC 1D8V(RT8209B)



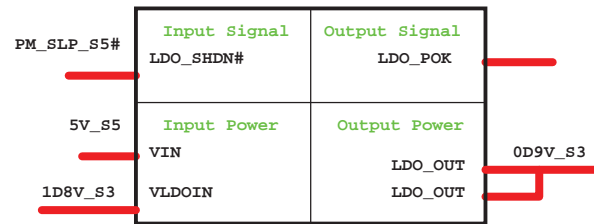
DCDC 1D1V(RT8209)



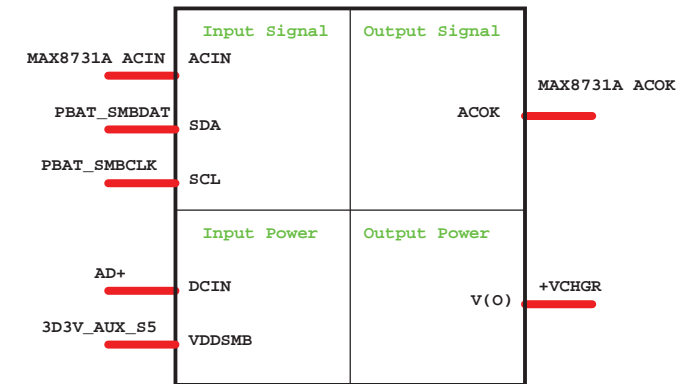
1D2V LDO G9161



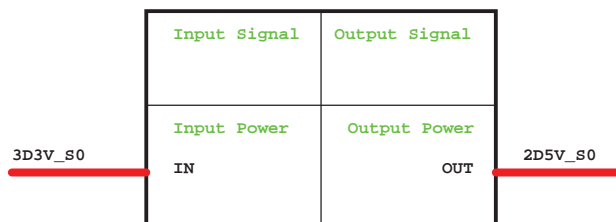
0D9V LDO RT9026



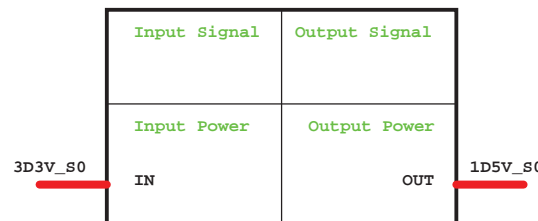
CHARGER MAX8731



2D5V LDO R9161



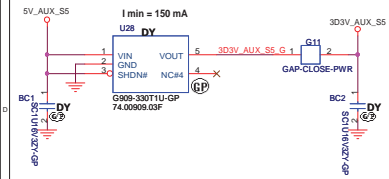
1D5V LDO G9571



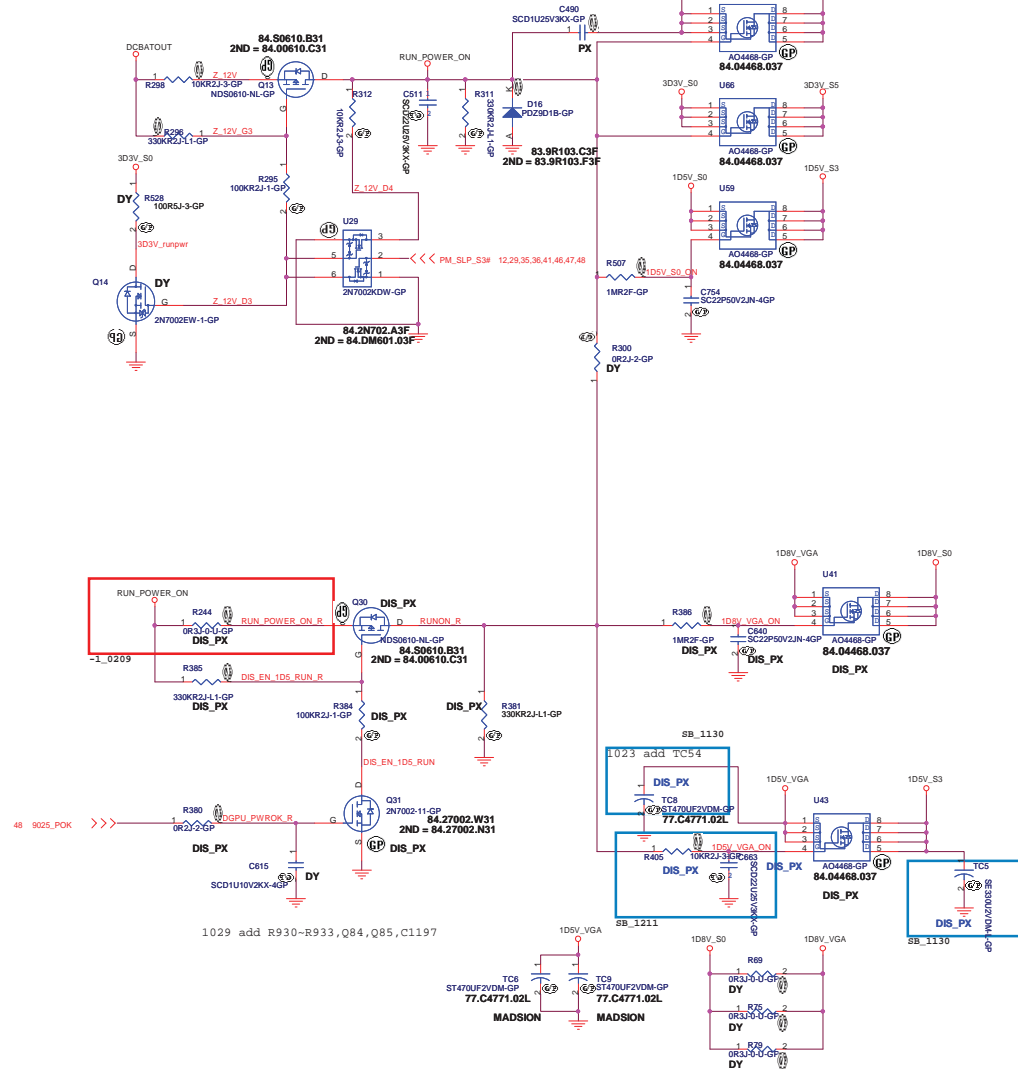
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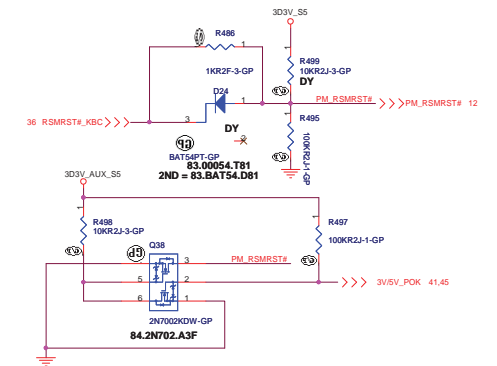
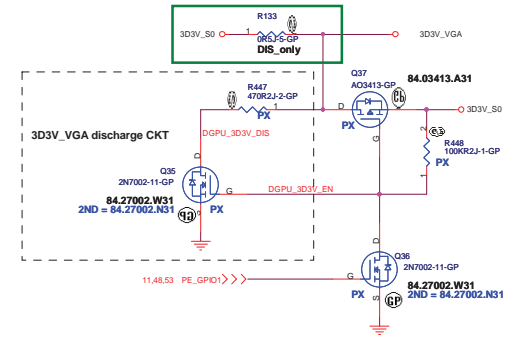
Title			Power Block Diagram		
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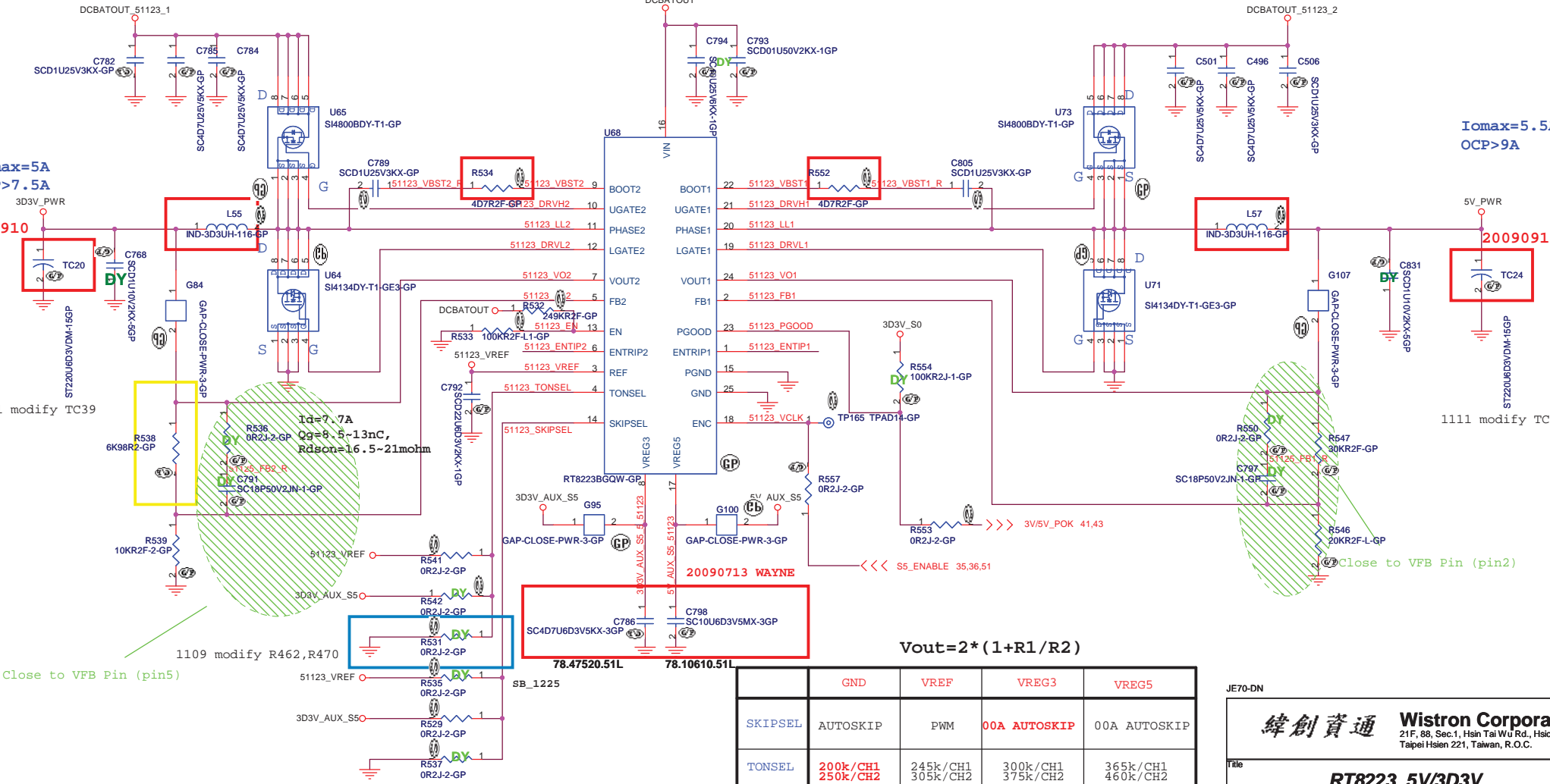
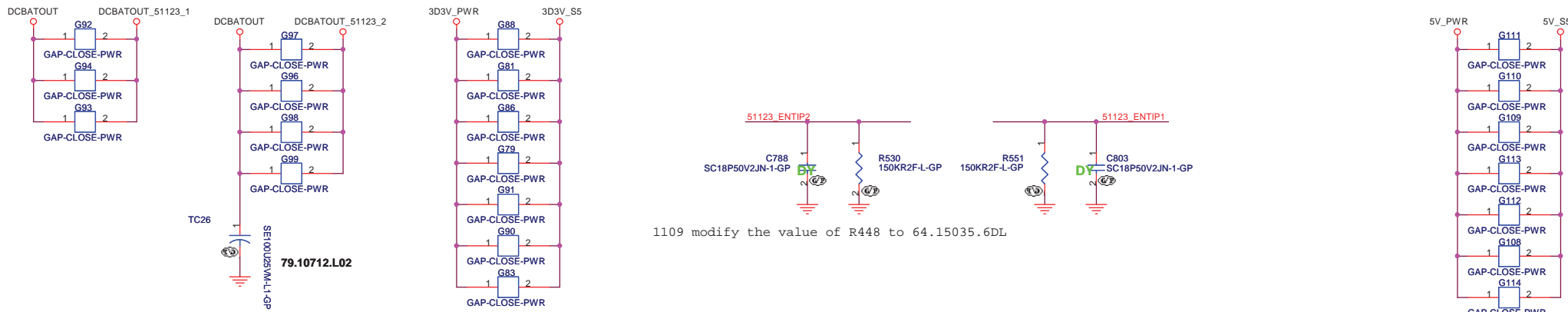


Run Power



+3VS to 3.3V_DELAY Transfer





	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

JE70-DN

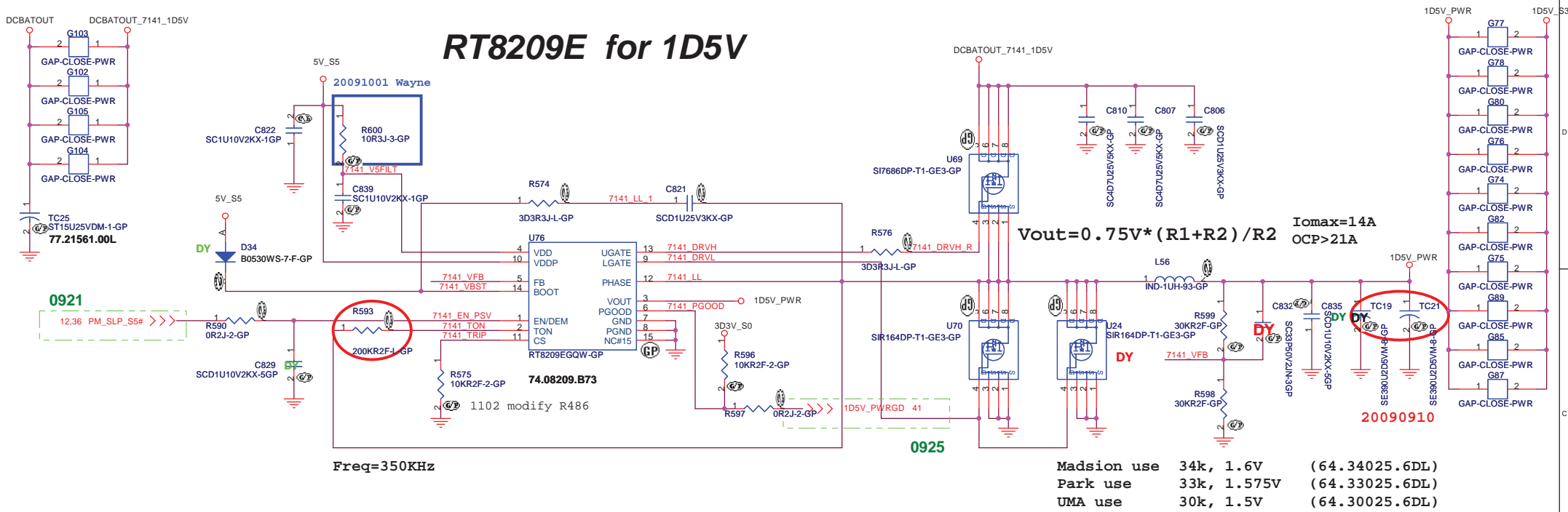
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8223 5V/3D3V**

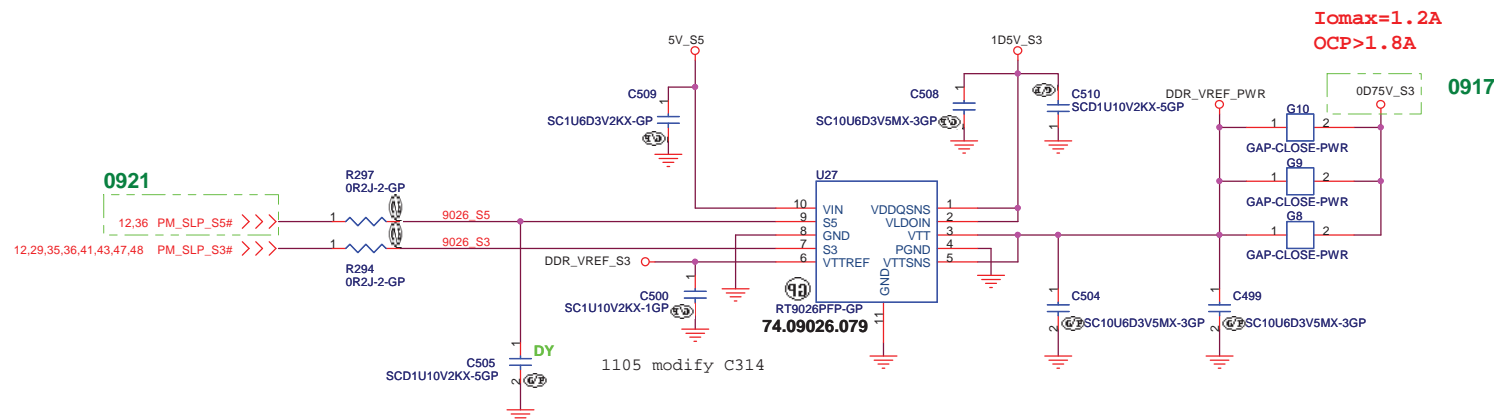
Size: Document Number **JE70-DN** Rev: **SB**

Date: Tuesday, February 23, 2010 Sheet 45 of 63

RT8209E for 1D5V

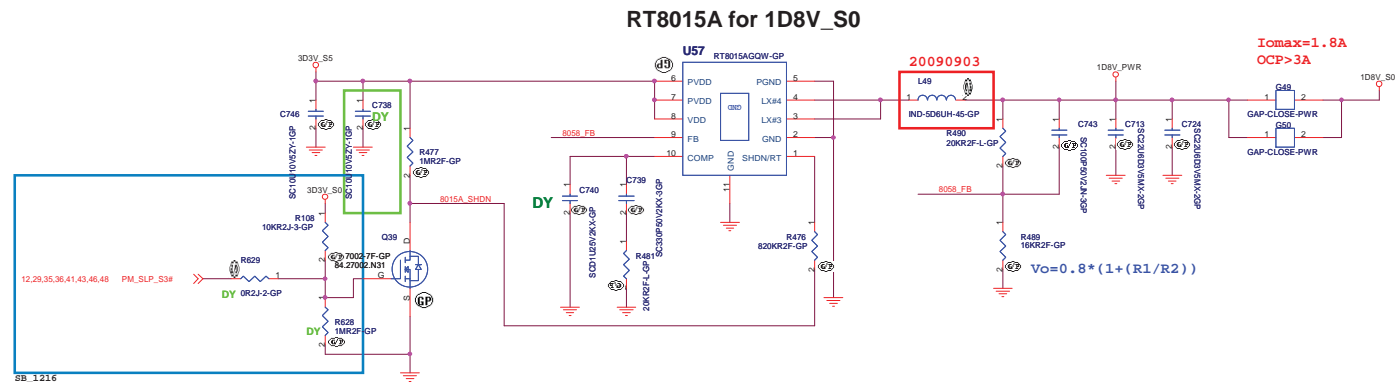
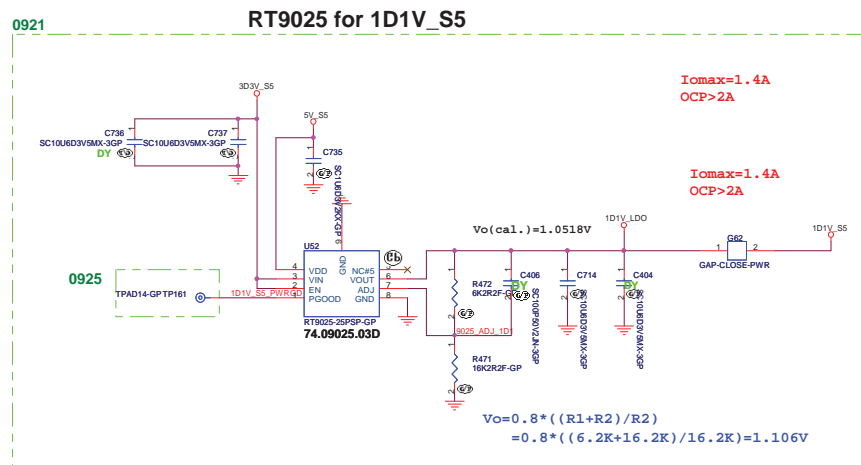
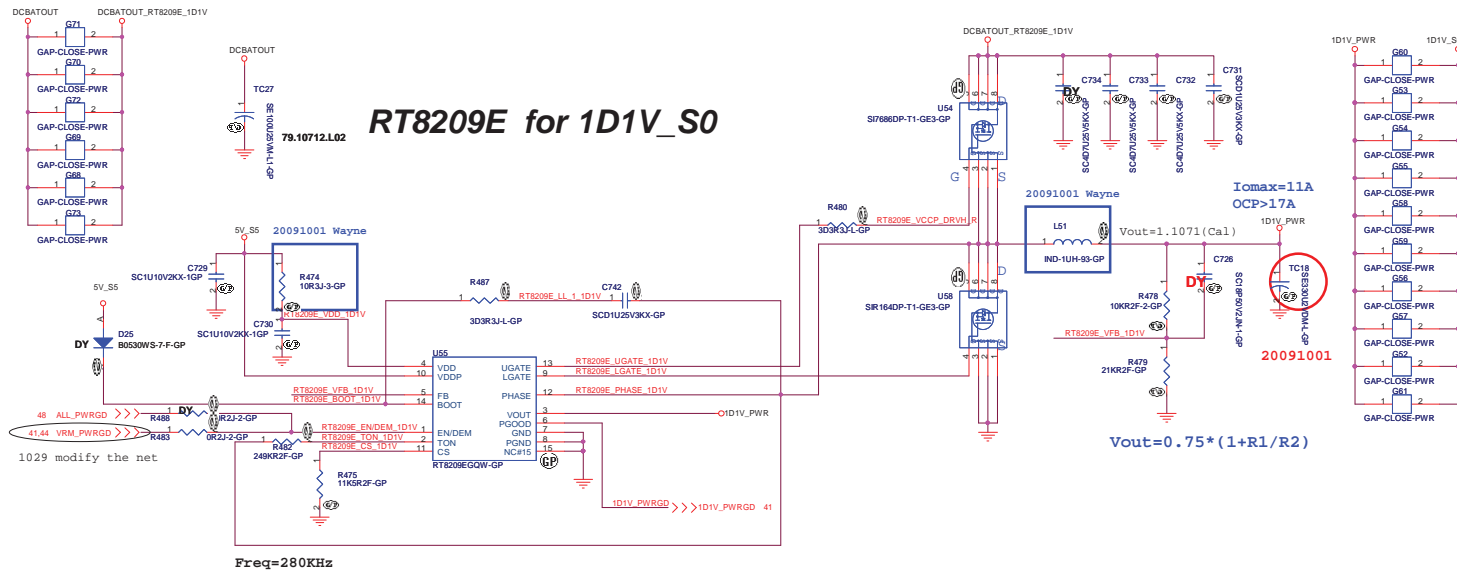


RT9026 for 0D75V_S3



JE70-DN

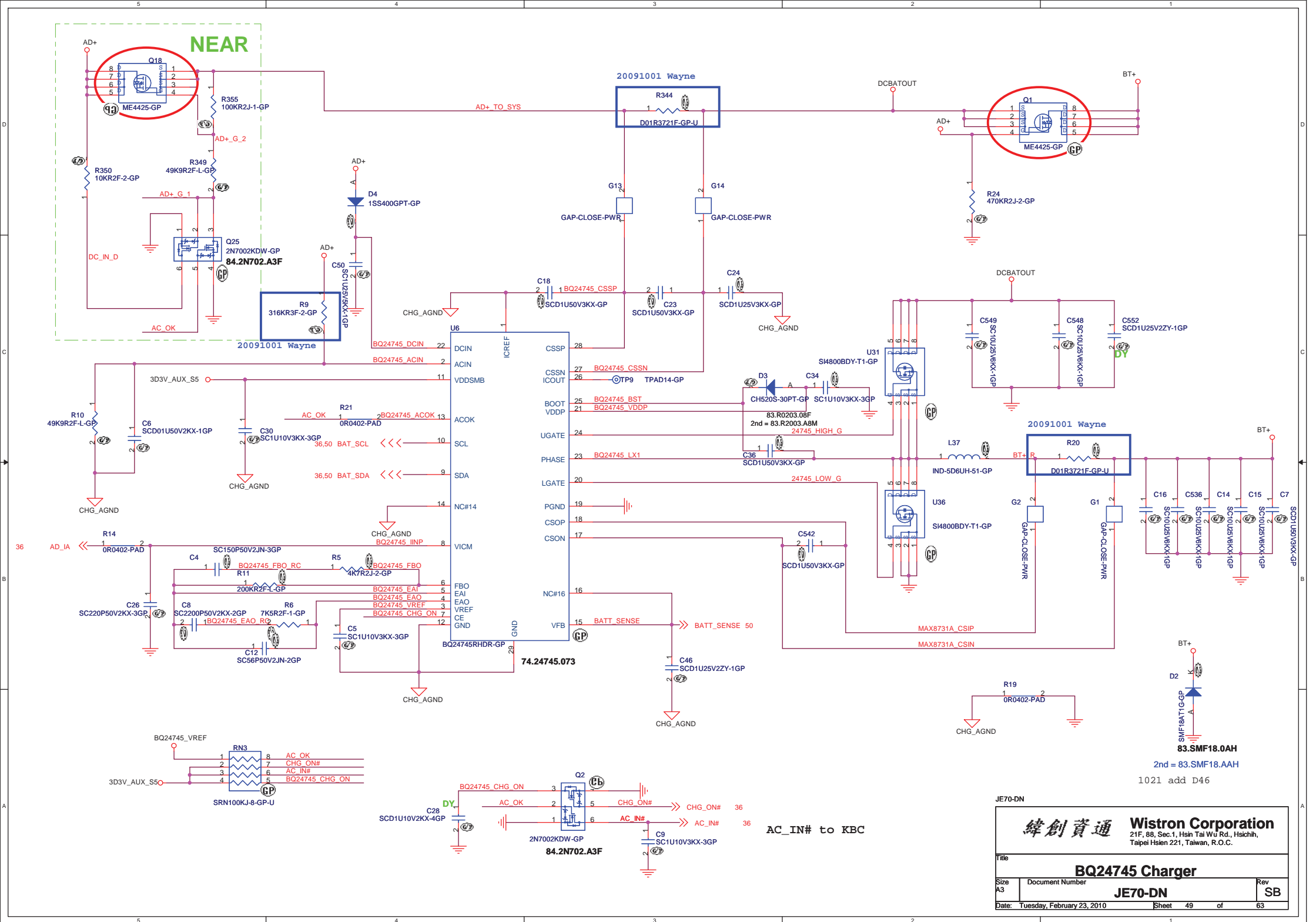
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: RT8209E 1D5V	
Size: Document Number	Rev: SB
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緯創資通 Wistron Corporation
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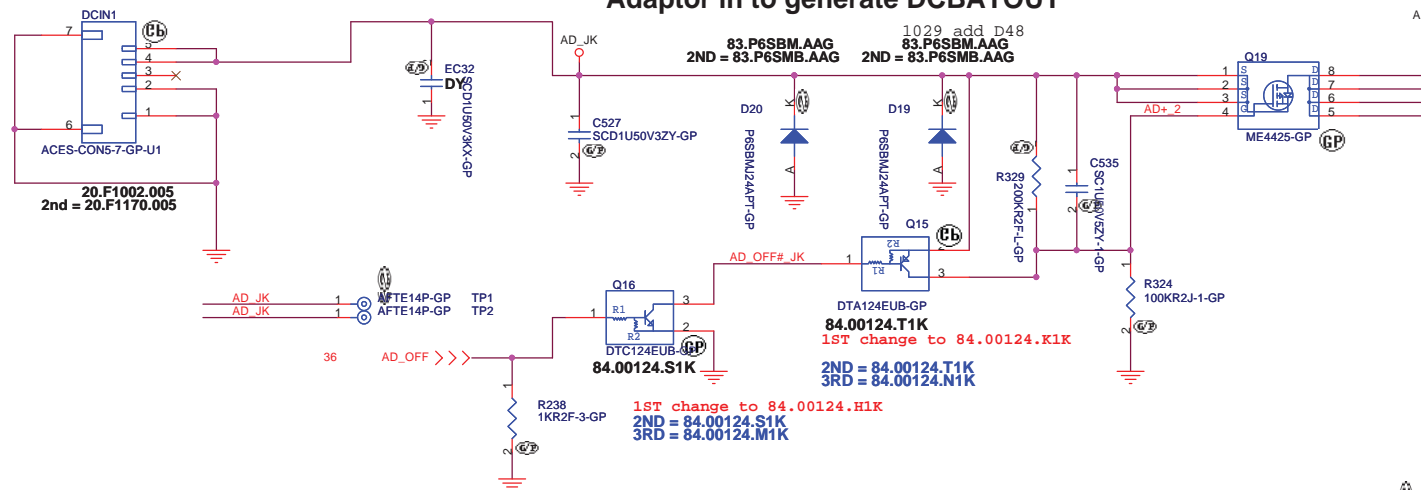
File	1D1V_S0 & 1D1V_S5 & 1D8V_S0
Size	Document Number
Rev	SB
Date	Monday, March 01, 2010
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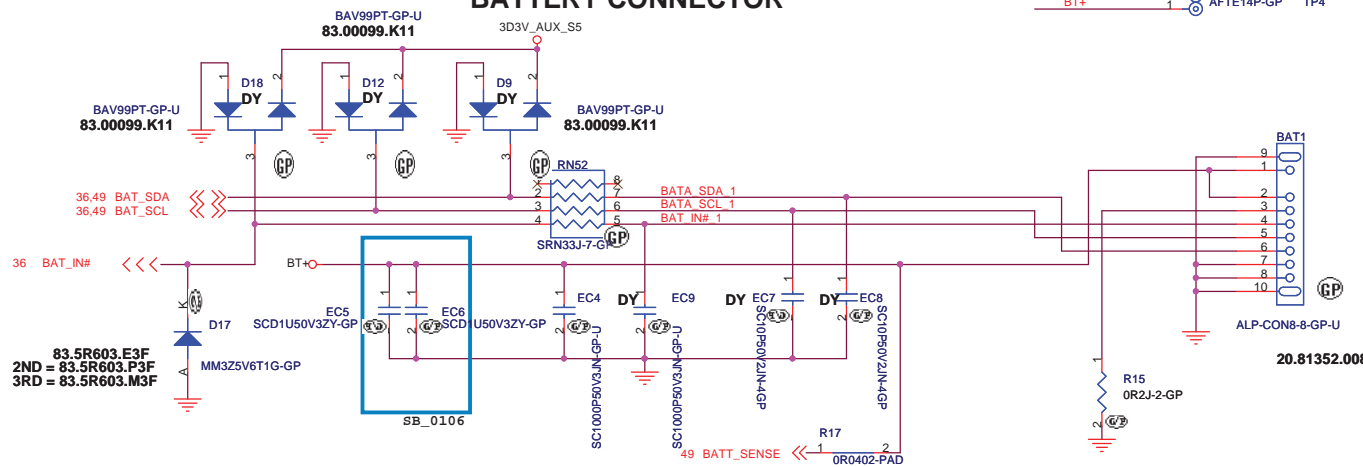
1Pin=3A

1021 modify DCIN1

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

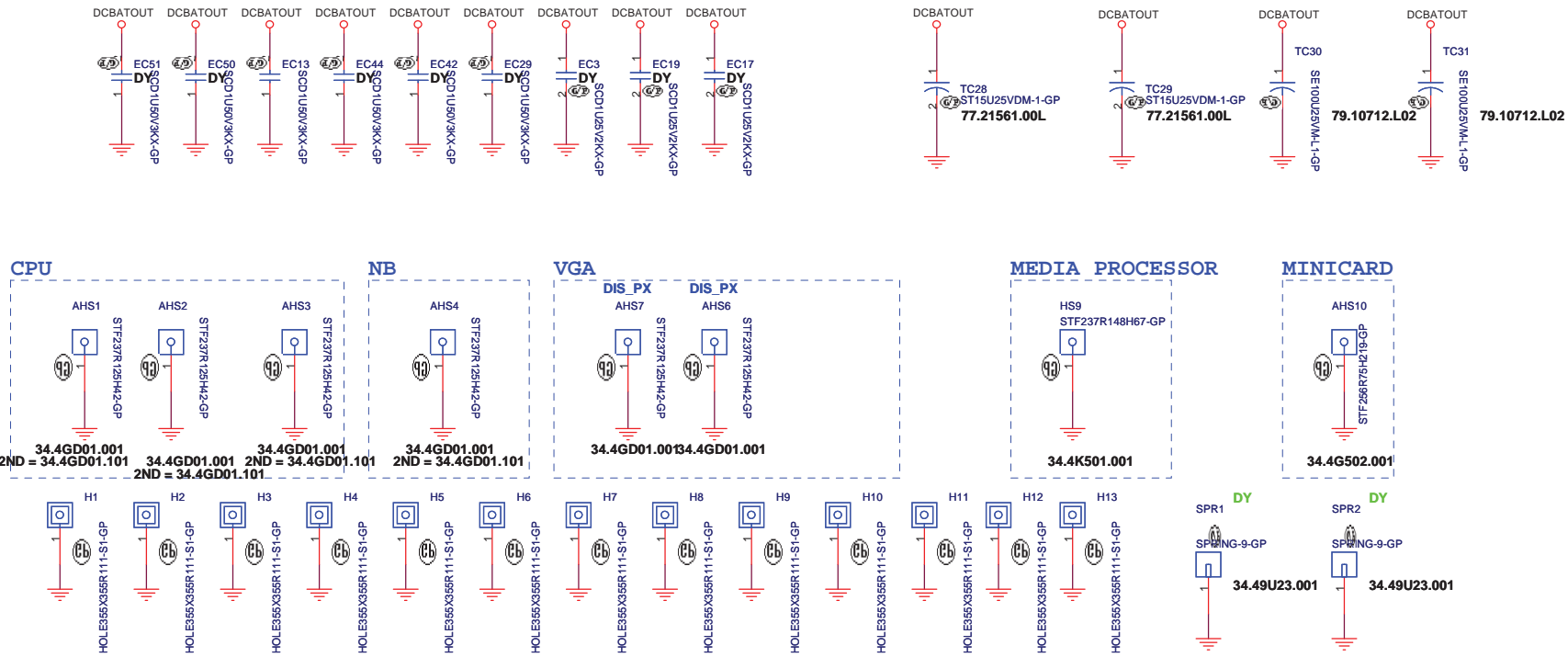


BATA_SDA_1	1	TE14P-GP	TP6
BATA_SCL_1	1	TE14P-GP	TP5
BAT_IN#_1	1	TE14P-GP	TP7
BT+	1	TE14P-GP	TP3
BT+	1	AFTE14P-GP	TP4

Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

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Check test point

3D3V_S0	TP171	TPAD14-GP
3D3V_AUX_S5	TP170	TPAD14-GP
3D3V_S5	TP172	TPAD14-GP
5V_S5	TP167	TPAD14-GP
12,36 PM_PWRBTN#	TP169	TPAD14-GP
6,11 CPU_PWRGD	TP163	TPAD14-GP
35,36,45 SS_ENABLE	TP173	TPAD14-GP
6,11 CPU_LDT_RST#	TP162	TPAD14-GP

Test Point放在Dimm Door打開可量測處

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Title

EMI/Spring/Boss

Size

Document Number

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Rev

SB

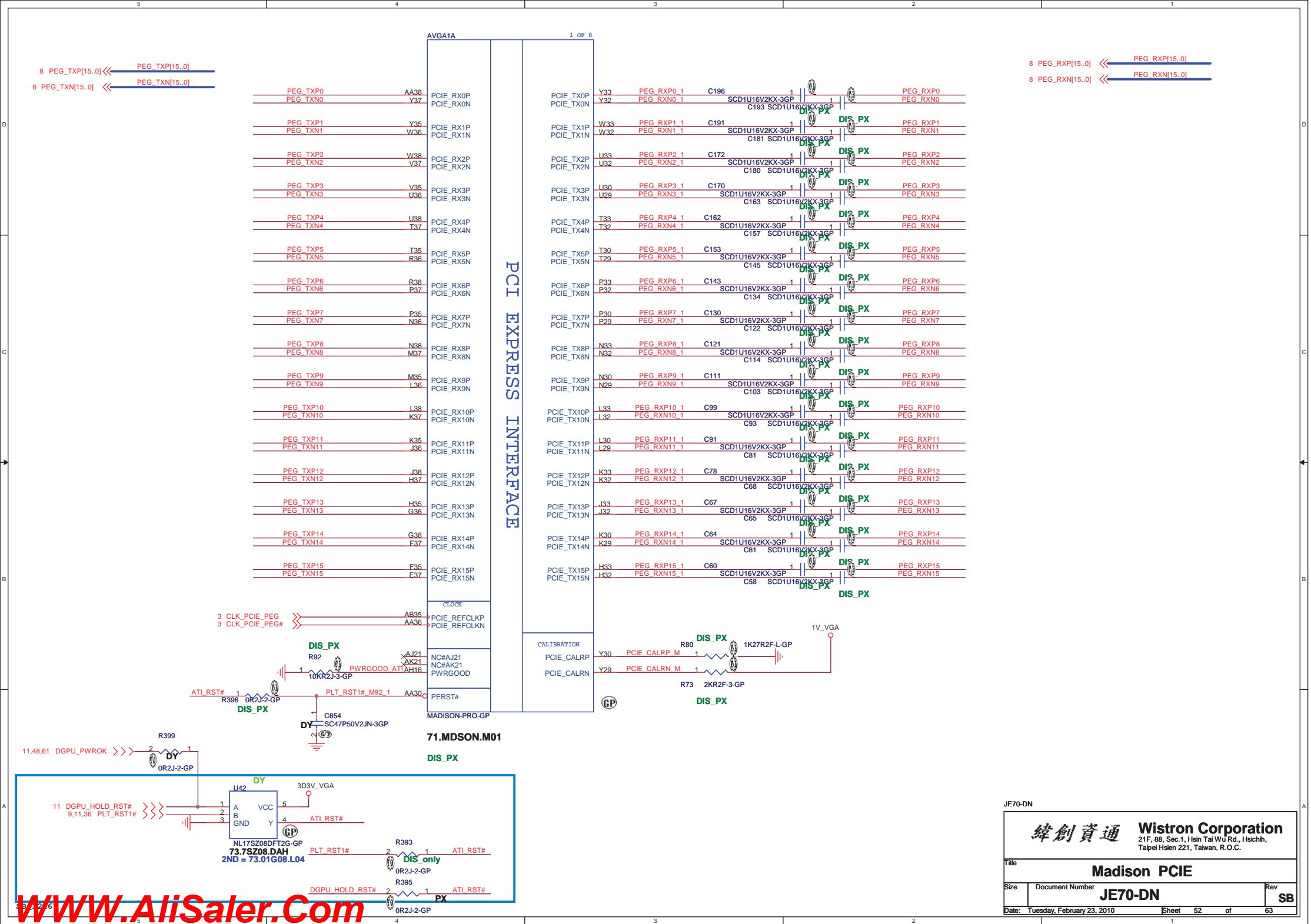
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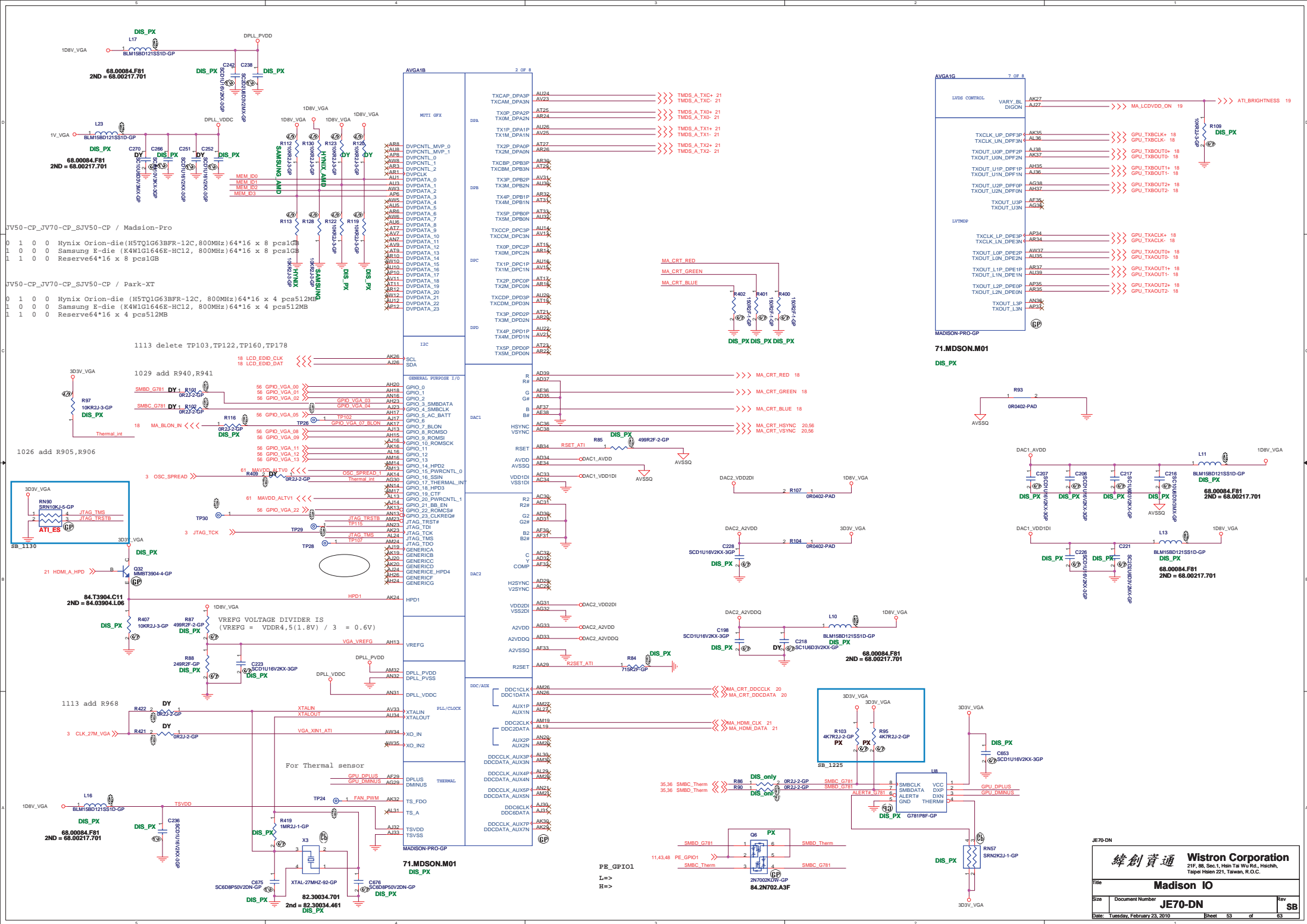
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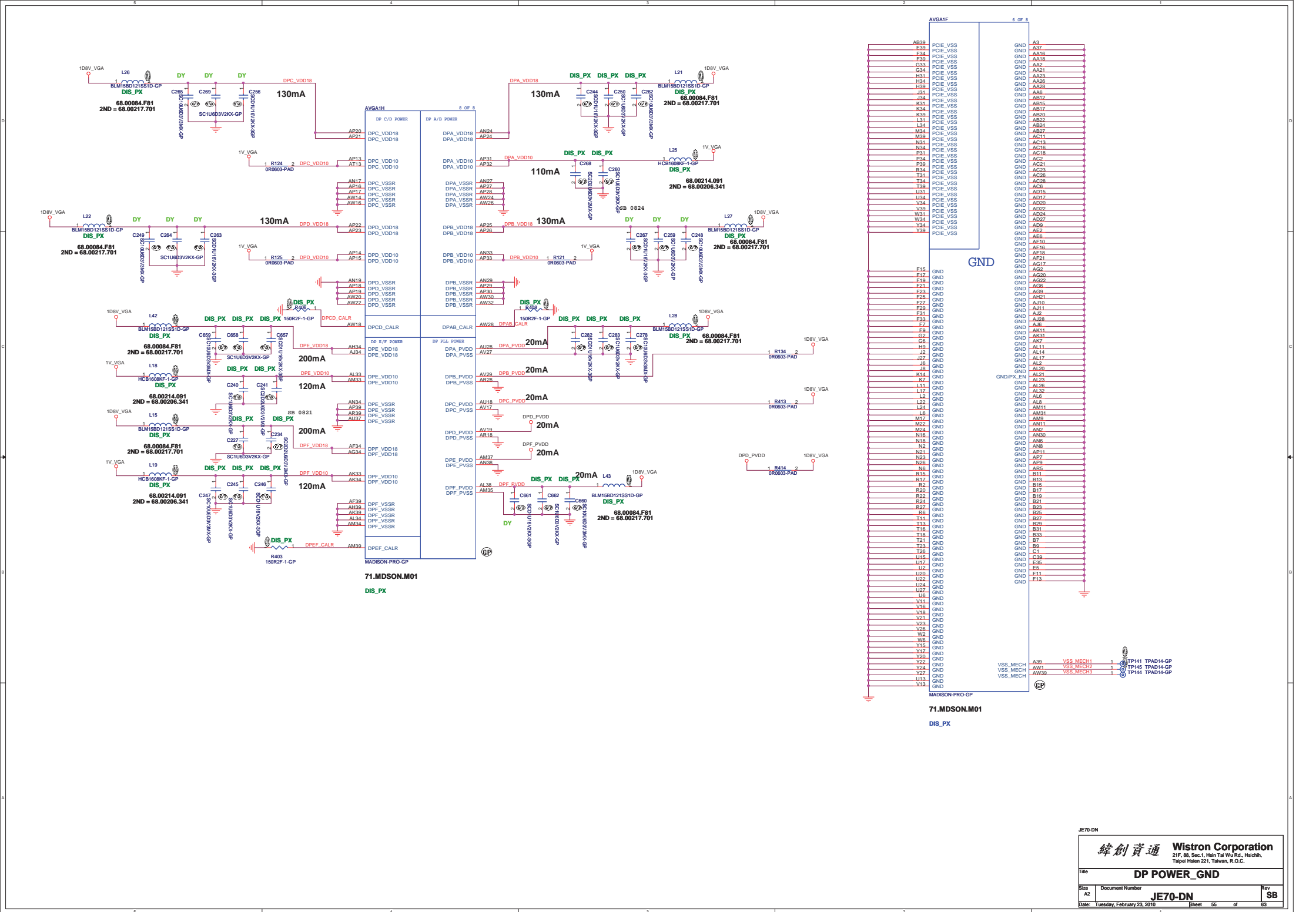
51

of

63







DDR3

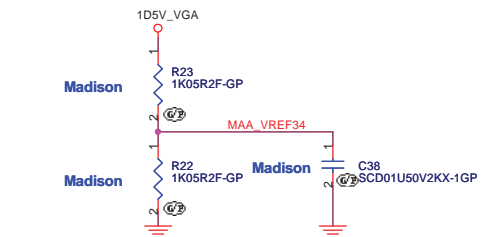
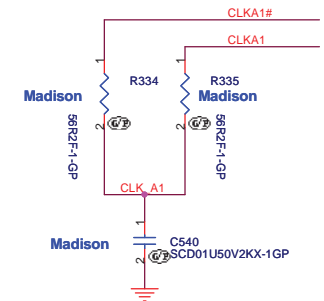


Madison
72.41164.H0U
2ND = 72.51G63.C0U

SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)



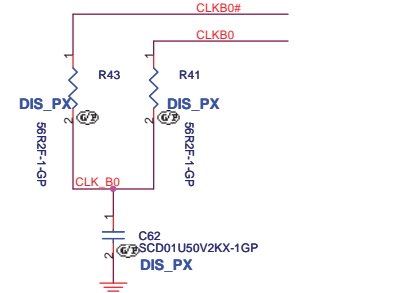
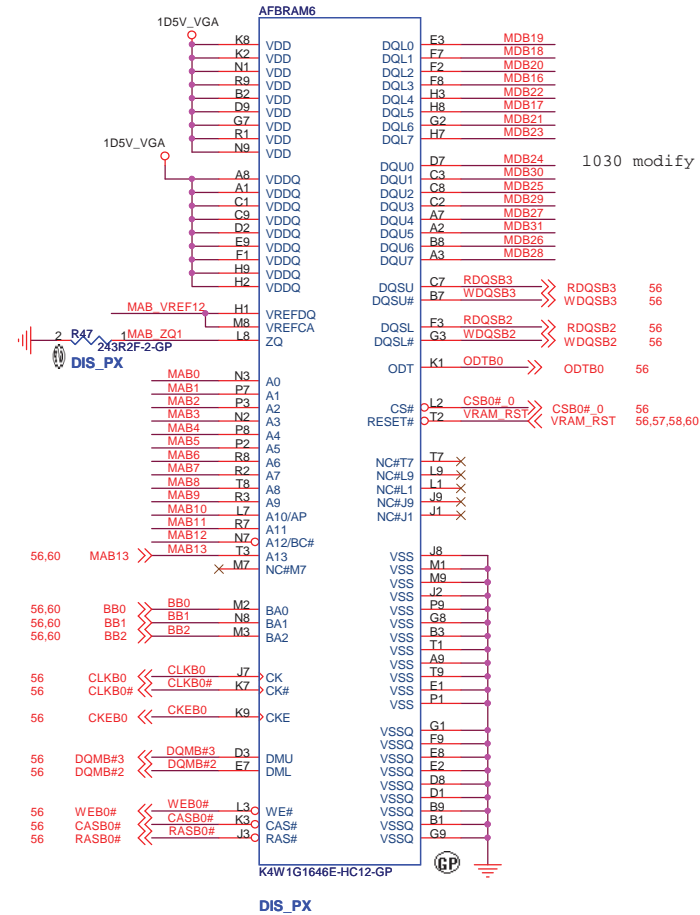
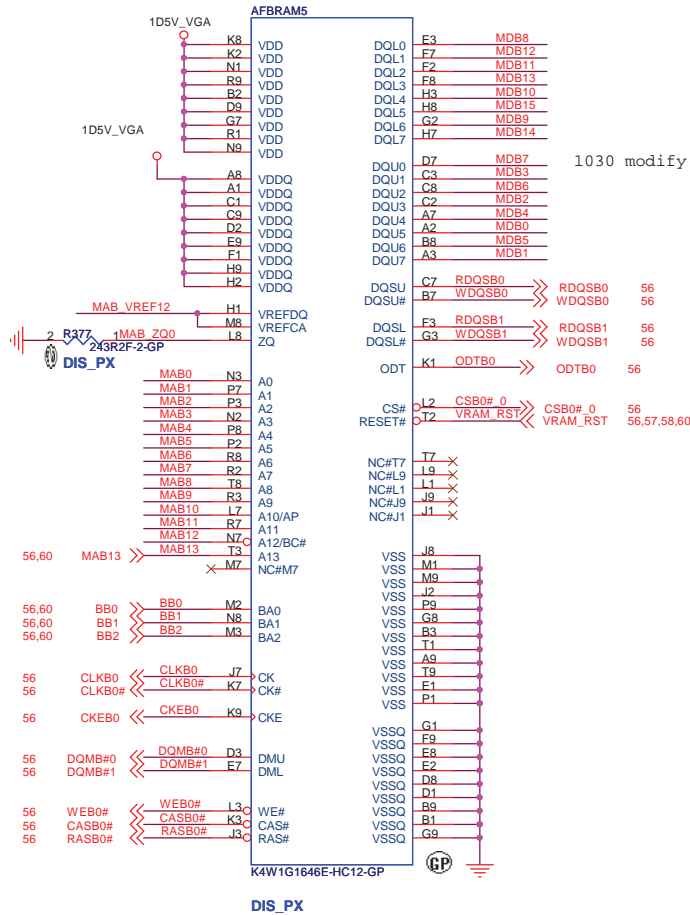
Madison
72.41164.H0U
2ND = 72.51G63.C0U



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Title			
VRAM(2/4)			
Size	Document Number	Rev	
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DDR3



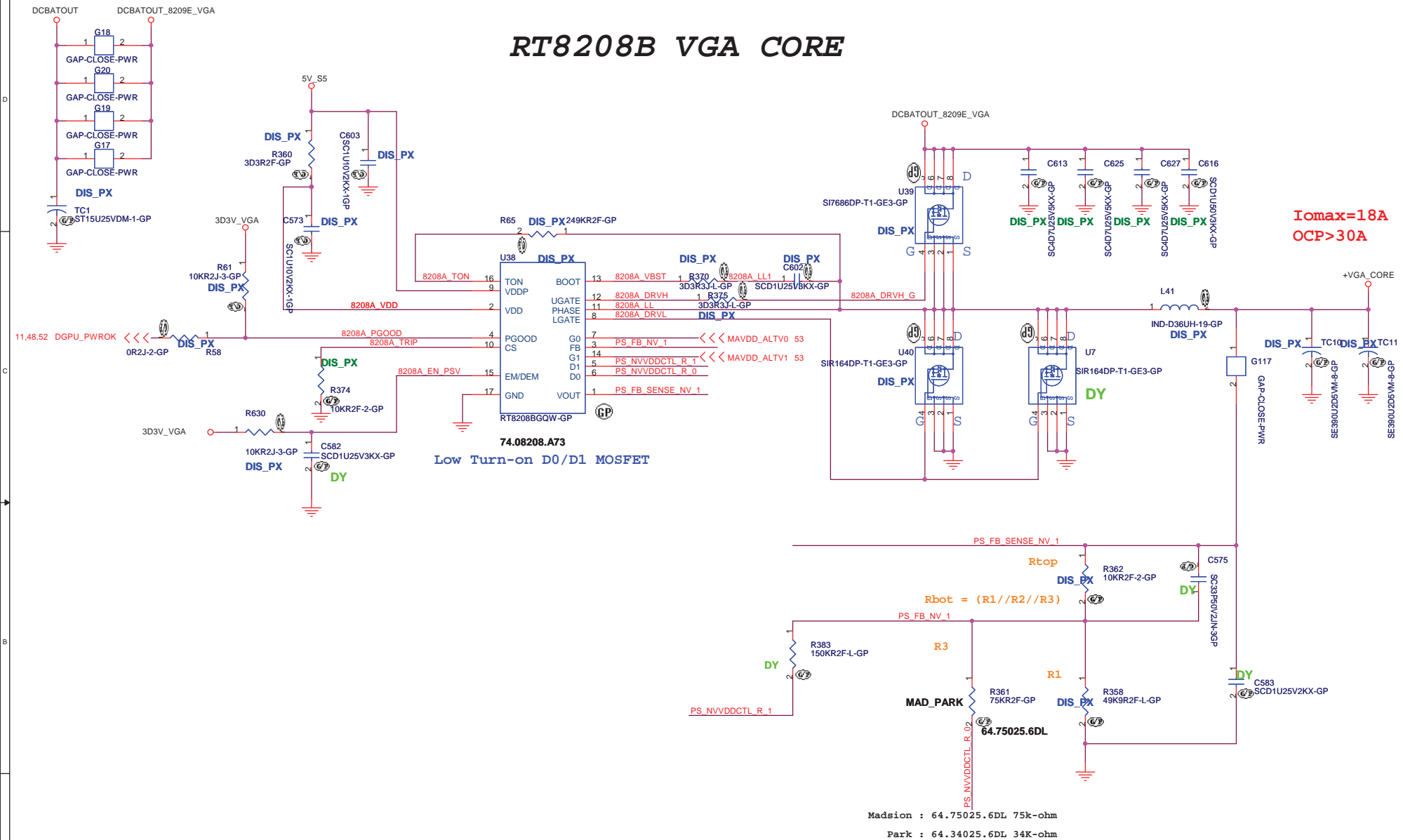
SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)

56,60 DQMB#[0..7] <<>>
56,60 RDQSB[0..7] <<>>
56,60 WDQSB[0..7] <<>>
56,60 MAB[0..12] <<>>
56,60 MDB[0..63] <<>>

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Title		
VRAM(3/4)		
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RT8208B VGA CORE



MAVDD_ALTVO	Madison Pro	Park XT
0	1.00V	1.12V
1	0.90V	0.90V

JE70-DN

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RT8209E_VGA_CORE

Size

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1020

Page8: modify these nets for PCIE ports
Page11: add these nets(INT_VGA_EN#,EDP_EN)
Page11: add the net(PX_EN#) and R861
Page11: delete D41,R437,R435
Page12: modify these nets for USB ports
Page14: modify L45,L48,L52,L57,L58,L60
Page18: delete RN95,R423 and add Q73-Q76,R862-R864,D45
Page19: delete CCD1 conn and modify these nets for CCD
Page19: add R865,R866,U100
Page20: add Q77,R867
Page24: add modify these nets for BT
Page25: add modify these nets for USB board
Page26: modify these nets for PCIE port(LAN)
Page26: delete the net(LOW_PWR)
Page33: modify these nets for PCIE ports(MINI1,MINI2)
Page33: modify these part's names
Page33: modify these nets for USB port(MINI2)
Page40: 1020 modify PWR_LED1,CHARGER_LED1
Page51: add screw holes

1021

Page5: modify these nets
Page6: delete HDT1 conn and add TP246~255
Page16: modify these nets of ADM1
Page16: add R880~883
Page17: modify these nets of ADM2 and ADM3
Page17: add R884~R891
Page18: add RN114~117
Page23: modify ODD1
Page25: modify the net(COVER_SW#_1)
Page30: modify LOUT1,AMIC1 and MICIN1
Page33: modify AMIN11 and MINI2
Page36: modify these nets and add R873~878
Page38: modify these devices(ATPCN1,SW_R,SW_L)
Page40: modify PWR_LED1,CHARGER_LED1
Page49: add D46
Page50: modify DCIN1, BAT1 and add R879

1021

Page26: modify U6(LAN IC)

1023

Page12: delete R538,R539 and add RN118
Page12: delete R442,R443,R445 and add RN119
Page12: delete R570-R572 and add RN120
Page12: delete C368-C371,C446,C449,C686,C687
Page18: swap these nets
Page21: add R892-R900,Q78
Page25: delete TC29,TC24,EC79,EC83
Page25: modify the net of USBCN1 pin32
Page36: delete R258 and RN89,RN122
Page36: delete R382 and add U101
Page36: delete R892,R483,R497,R478 and add RN123
Page36: delete R410,R416 and add RN121,R892
Page37: add R901,R902
Page40: modify the pin5 define of PWR_CN1 and Q11
Page43: add TC53,TC54,U44
Page61: modify TC52, R295 and add R903,Q79

1026

Page3: add R904 and modify C509,R232,R235
Page6: add R913,RN124
Page6: modify RN42,RN84,R612,R611,R364
Page17: modify these nets
Page19: modify R588
Page21: modify U73 and delete R504
Page22: modify SATA1
Page35: delete R311 and modify FAN1
Page36: modify RN121
Page36: modify AKB1
Page37: modify RN94 and the net(SPI_WF#)
Page43: add R097-R911,D47,Q80
Page53: add R905,R906

1027

Page10: delete C651,R320,R316
Page11: modify C543,C306,C424,C433
Page11: delete R148
Page12: modify the net(PM_RSMRST#)
Page43: modify the net(PM_RSMRST#)

1028

Page3: add the net(LAN_CLKREQ#) to RN70
Page4: modify C704-C706
Page4: modify R401
Page9: delete R576,R578
Page10: modify C62,C91
Page11: delete R207,C337,D5,R208
Page11: delete the net(PCI_REQ#6)
Page12: delete RN120 and add R570
Page13: modify the net(SATA_LED#)
Page14: add C1198,C1199 and modify C815,C811
Page16: add R934,R935
Page18: add U102,R915-R919
Page18: modify R432,U3,U8
Page19: add U103,R920-R922 and delete D35
Page20: add R936,R937 and modify R325,R323,R354
Page21: delete RN8,RN13,RN15,RN19
Page21: modify C819-C821,C823,C824,C826-C828
Page25: add L82,R924,R925
Page29: modify R489
Page30: modify R622,R619 and add RN125
Page36: delete R384 and modify the net(KBC_BL_ON_IN)
Page36: add R926
Page43: delete R583,D33,U74,R340,Q34,R584
Page43: add R930-R933,Q84,Q85,C1197
Page43: add R927-R929,Q8-Q83
Page43: delete R591-R595
Page48: modify these nets(DGPU_PWROK,9025_POK)

1029

Page6: delete R364,R612 and add RN127,R946
Page16: delete C331,C338
Page17: delete C348,C340,C350,C342
Page18: modify these nets
Page19: add EC99,EC100
Page24: add EC101,EC102
Page25: add L82,R924,R925,R939,EC103
Page35: delete D17,D18,U39,U43,R298,R322,R330,R338,R337,C646,C656
Page35: delete U38,R321,R308,R309,R314,C645
Page36: add R945,RN126
Page43: delete U44,R342,C675
Page47: modify the net
Page48: modify R582 and add R938
Page50: add D48
Page53: add R940-R943
Page61: add R944,Q86

1030

Page3: modify these nets
Page8: modify these nets
Page11: modify the net
Page12: add R949
Page14: delete C760,C721,C805,C800,C769,L64 and add R948
Page18: modify these nets
Page30: add R950-R953 and modify EC24,EC51
Page57: swap these nets
Page58: swap these nets
Page59: swap these nets
Page60: swap these nets

1102

Page3: swap these nets
Page6: swap these nets
Page12: swap these nets
Page13: swap these nets
Page18: swap these nets
Page25: modify USBCN1
Page30: modify these names of these nets

1103

Page3: modify X5,C508,C509
Page11: modify R164
Page14: modify L51,L59
Page21: modify these names of nets
Page21: add RN8,RN13,RN15,RN19
Page36: add the net(A_MIC_SUPPORT#)

1104

Page6: delete TP246~255 and add HDT1
Page9: modify the value of RN11
Page24: add AFTP(TP256-TP258)
Page24: add AFTP(TP259-TP263)
Page25: add AFTP(TP264-TP280)
Page35: add AFTP(TP281,TP282)
Page36: add AFTP(TP283-TP307)
Page38: add AFTP(TP308-TP312)
Page40: add AFTP(TP313-TP319)
Page56: modify these values of R724,R725

1105

Page3: delete R191-R194,R198-R200,R204-R206
Page3: delete R214,R213,R187-R190,R220,R222
Page3: add RN128-RN136
Page3: modify R215,R197,R238,R229
Page6: delete R104,R105,R108,R110
Page6: add RN137,RN138,R954
Page6: modify R366
Page6: modify Q8,R81,R375,C205
Page8: delete TP16,TP17,TP20,TP21
Page9: add R955,R956 and modify R29
Page11: delete R144,R141,R137,R138
Page12: add the net(SUS_STAT#) and R957
Page12: modify these nets
Page21: swap these nets
Page28: modify C713,R634 and delete R626
Page33: modify these nets
Page33: modify R879

1106

Page3: modify these values of R169,R170
Page12: add R957,R958
Page12: add these nets(USB_OC#0,USB_OC#2,USB_OC#3)
Page16: modify R880-R883,ADM1
Page17: modify R888,R890,ADM2
Page21: add R959
Page35: modify FAN1
Page35: modify PWR_CN1
Page35: modify ATPCN1
Page36: swap these nets(KBRCIN#,KA20GATE)
Page37: swap RN94
Page44: swap RN45
Page51: add EC104-EC112 for EMI demand

1107

Page3: swap RN129,RN130,RN132
Page6: swap RN137
Page51: add EC104-EC112 for EMI demand

1109

Page45: modify the value of R448 to 64.15035.6DL for Power team demand
Page45: modify R462,R470 for Power team demand
Page46: modify L25 for Power team demand
Page48: modify C1032,C1194

1110

Page5: swap RN48
Page7: add C1200-C1207
Page11: add R960,R961
Page25: modify USB1
Page43: add TC55,TC56
Page52: add R962

1111

Page11: add R965
Page21: modify HDM11
Page28: add R626
Page33: delete C550,C549 and add R963
Page36: delete RN121 and add R964
Page45: modify TC39,TC40
Page48: add R966,Q87,C1208,R967,R968,Q88

1112

Page13: modify the net
Page48: delete R968,Q88
Page48: modify R819,R820,R966
Page48: modify the net

1113

Page3: delete R170,EC50
Page25: delete R939,TP272,EC103
Page46: modify TC43
Page48: add R969
Page53: add R968
Page53: delete TP103,TP122,TP160,TP178
Page53: delete these TP(TP157,TP145...))
Page54: delete TP3-TP9

1117(Rename)

Page18: swap these nets
Page22: delete D29-D31,D33
Page36: modify RN31
Page61: delete G24-G29
Page61: modify the net

1118

Page14: add R620 and modify R184
Page15: modify R412,R411
Page36: swap AKB1 pin1-pin26

SA to SB

1120

Page19: modify these nets
Page48: modify the net(9025_EN)

1124

Page38: modify ATPCN1

1126

Page25: modify these nets
Page36: add TP174